DEDF'2012

# "*Патентная защита цифровой микро-электроники*"

**SoftPatent**

TechTunnel

# Зачем компании патенты?

- Единственный инструмент защиты R&D
- Инструмент цивилизованной продажи R&D
- Единственный способ продать R&D задорого
- РФ: Инструмент финансового управления
- РФ: Инструмент защиты бизнеса от рейдеров

# Как патентуется цифровая микро-электроника

US005790062A

# United States Patent [19]

Darnell et al.

[11] Patent Number: 5,790,062

[45] Date of Patent: Aug. 4, 1998

[54] **DELTA MODULATOR WITH PSEUDO CONSTANT MODULATION LEVEL**

[75] Inventors: **Brad Darnell**, San Jose; **Rouben Toumani**; **Paul Bauer**, both of Morgan Hill, all of Calif.

[73] Assignee: **Wiltron Company**, Morgan Hill, Calif.

[21] Appl. No.: **653,933**

[22] Filed: **May 23, 1996**

[51] **Int. Cl.**[6] ..... **H03K 13/00**

[52] **U.S. Cl.** ..... **341/143**; 375/242

[58] **Field of Search** ..... 341/143, 144, 341/155; 375/242, 243, 250–254

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| 4,646,322 | 2/1987 | Flanagin et al. | 375/27 |
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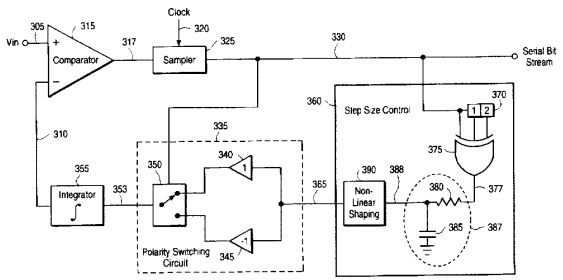
*Assistant Examiner*—Peguy JeanPierre
*Attorney, Agent, or Firm*—Fliesler, Dubb, Meyer & Lovejoy

[57] **ABSTRACT**

The present invention is directed to delta modulation in which the modulation level is optimized to improve overall system performance. A delta modulator in accordance with the invention includes a step size controller having a overload detector, a step size generator and a modulation level regulator. The overload detector monitors the output serial bit stream and produces a signal indicative of whether overload conditions are present. The step size generator produces steps of varying sizes in response to an input signal. The modulation level regulator monitors the signal output from the overload detector and outputs a modulated signal when the overload detector output has reached at least a certain threshold level. The modulation level regulator output is received at the step size generator input.

**37 Claims, 31 Drawing Sheets**



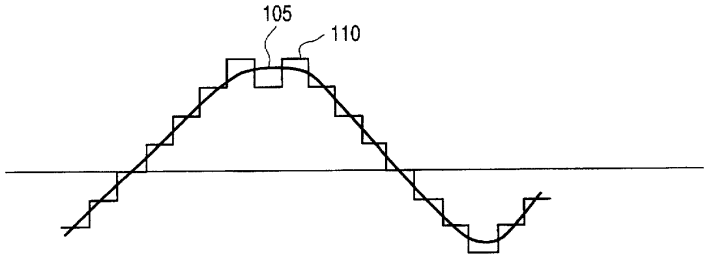



FIG. 1
(PRIOR ART)

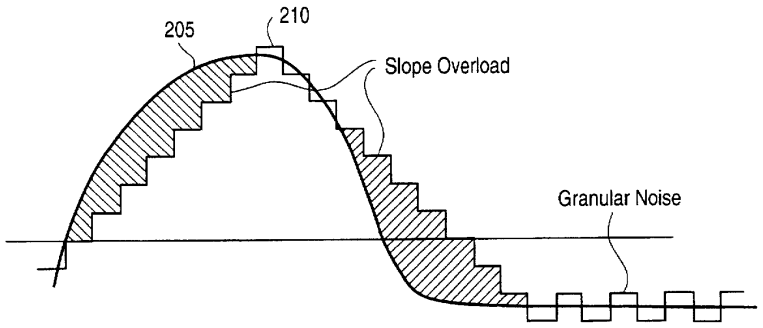



FIG. 2
(PRIOR ART)

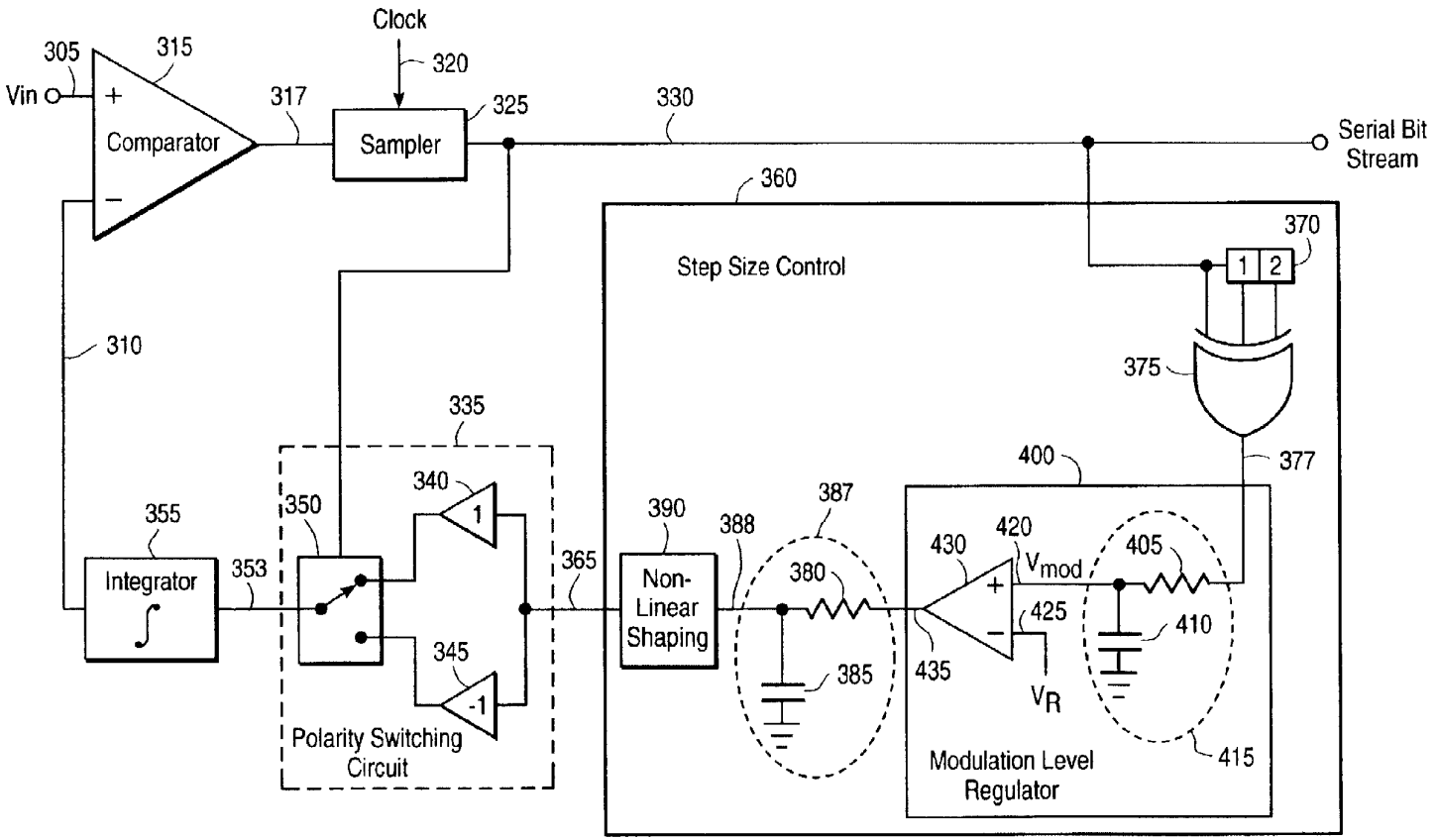
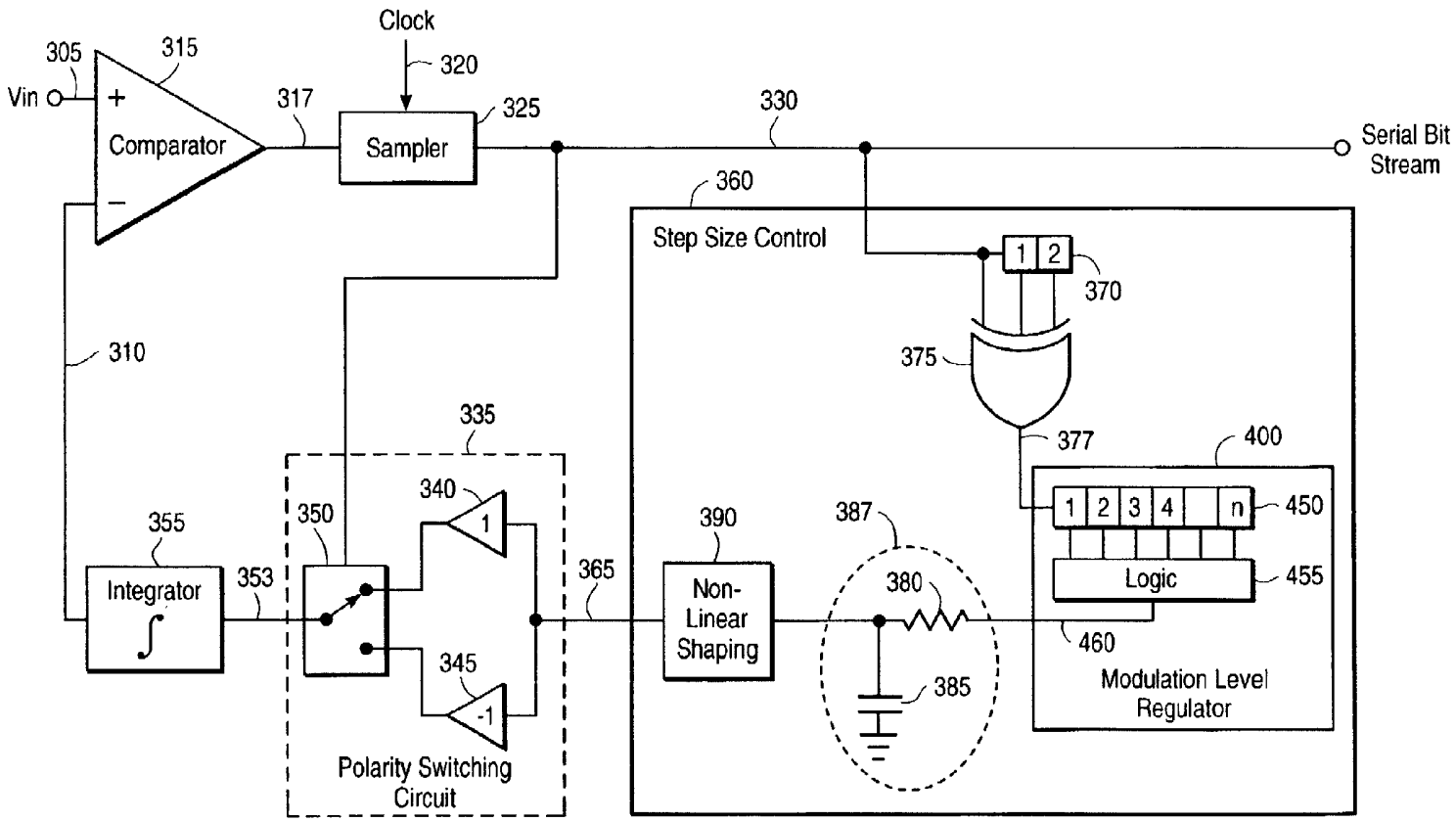

Clock
320
305
315
Vin
+
Comparator
−
317
Sampler
325
330
Serial Bit Stream
360
Step Size Control
370
1
2
375
377
400
310
335
340
1
350
355
Integrator
353
345
-1
Polarity Switching Circuit
365
390
Non-Linear Shaping
388
387
380
385
430
420
Vmod
425
435
VR
405
410
415
Modulation Level Regulator

FIG. 6


Clock
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Vin
+
Comparator
−
317
Sampler
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Serial Bit Stream
360
Step Size Control
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2
370
375
377
400
310
335
340
1
350
355
Integrator
353
345
-1
Polarity Switching Circuit
365
390
Non-Linear Shaping
387
380
385
1
2
3
4
n
450
Logic
455
460
Modulation Level Regulator

FIG. 7

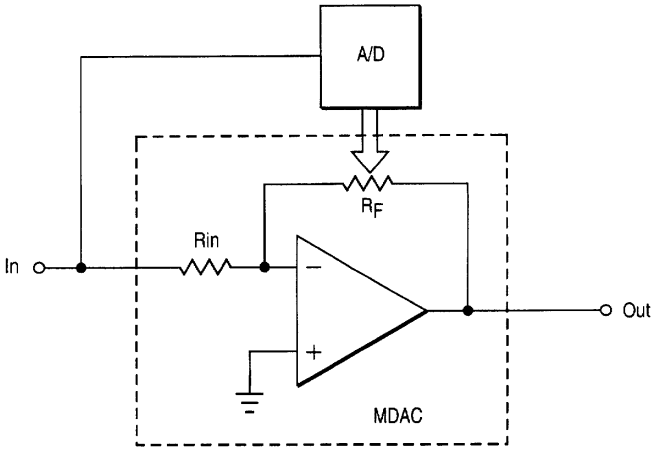



FIG. 9a

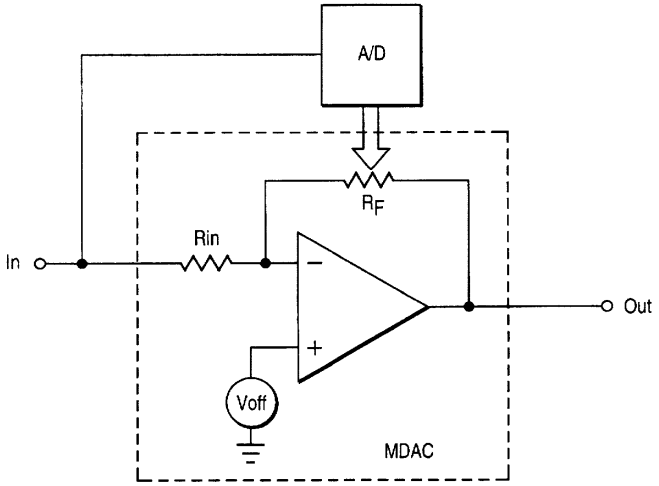
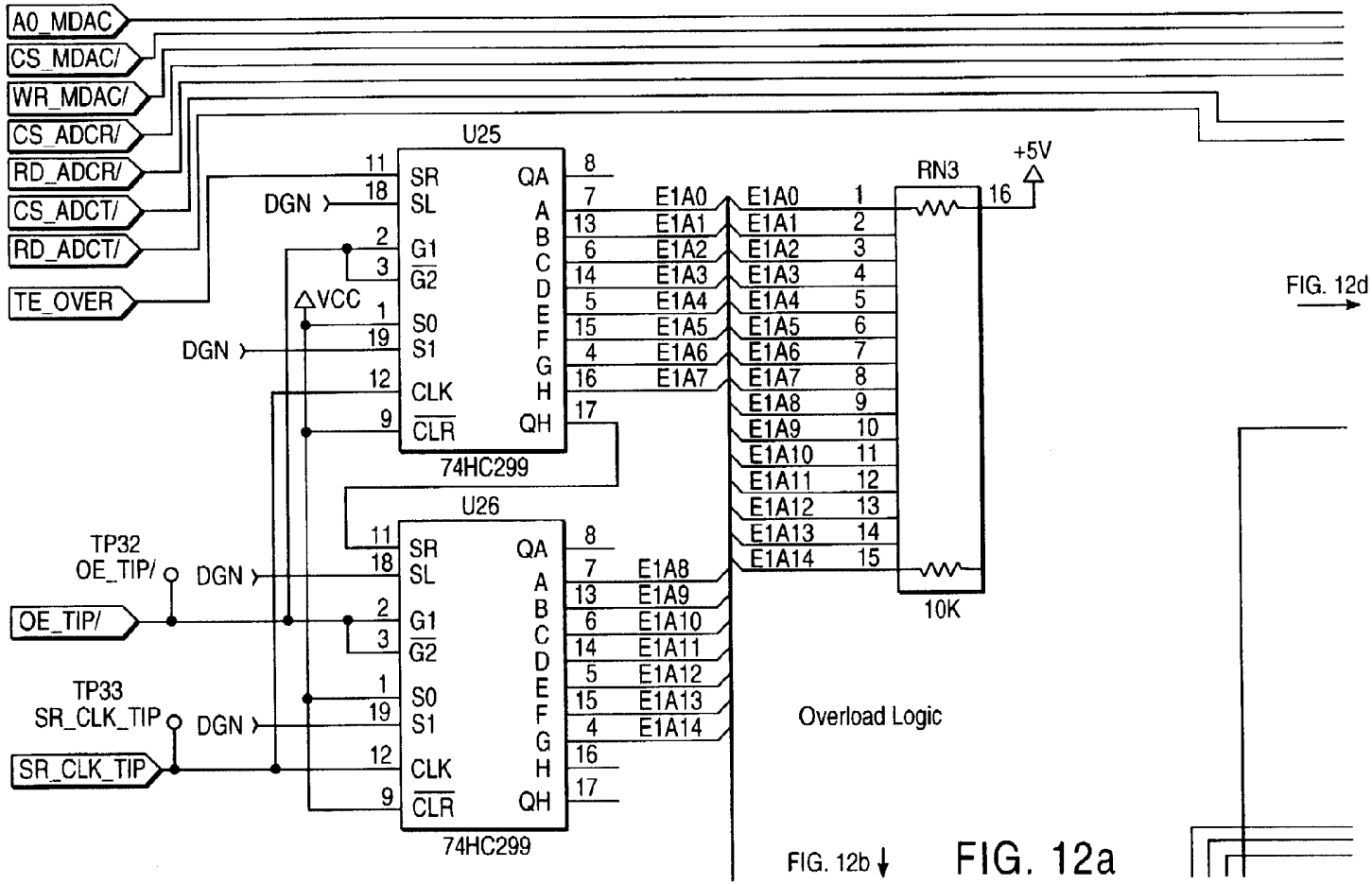



FIG. 9b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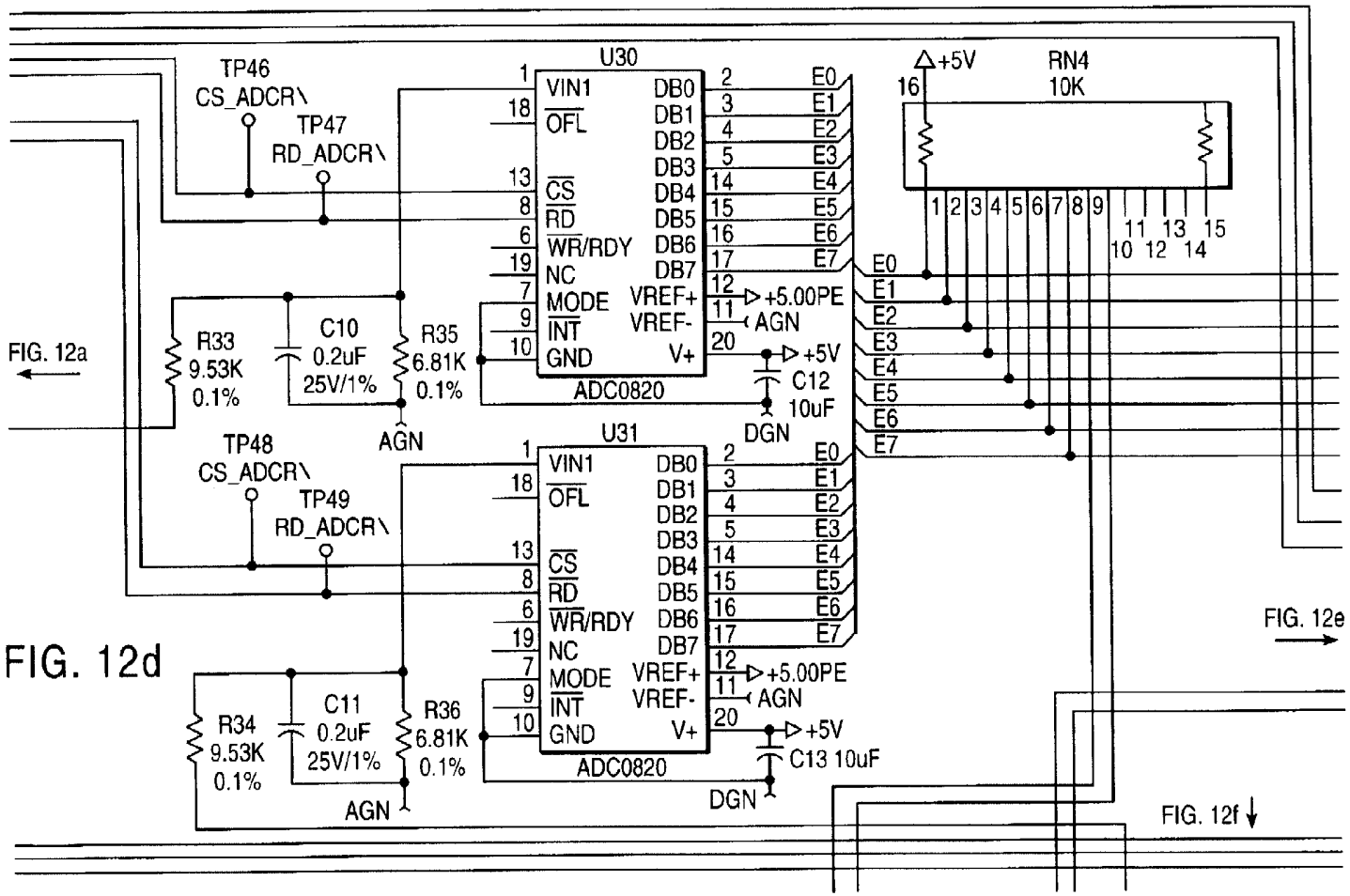
SR
SL
G1
G2
S0
S1
CLK
CLR
QA
A
B
C
D
E
F
G
H
QH
DGN
VCC
+5V
RN3
10K
E1A0
E1A1
E1A2
E1A3
E1A4
E1A5
E1A6
E1A7
E1A8
E1A9
E1A10
E1A11
E1A12
E1A13
E1A14
TP32
OE_TIP/
TP33
SR_CLK_TIP
Overload Logic
FIG. 12d
FIG. 12b
FIG. 12a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TP47
RD_ADCR\
U30
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OFL
CS
RD
WR/RDY
NC
MODE
INT
GND
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
VREF+
VREF-
V+
ADC0820
+5.00PE
AGN
+5V
C12
10uF
DGN
E0
E1
E2
E3
E4
E5
E6
E7
+5V
RN4
10K
R33
9.53K
0.1%
C10
0.2uF
25V/1%
R35
6.81K
0.1%
AGN
FIG. 12a
TP48
CS_ADCR\
TP49
RD_ADCR\
U31
R34
9.53K
0.1%
C11
0.2uF
25V/1%
R36
6.81K
0.1%
C13 10uF
FIG. 12d
FIG. 12e
FIG. 12f

```
short scan(unsigned int value, short criteria) short i,count;
unsigned int mask;
count = 0;
mask = 0x0001;
for (i = 0; i < 12; i++) { if (value & mask) count ++;
mask <<= 1;
} return (count >= criteria); }
/*****************************************************/
int main (int argc, char * argv []) { FILE *outf; BIT.sub.-- FILE
*outfile; unsigned int iter,max.sub.-- iter,linecount,j;
 outf = fopen("pigrom4.asc","wt");
if (outfile = OpenOutputBitFile ("pigrom4.dat")) { max.sub.--
inter = 0x7fff; for (iter = 0; iter <= max.sub.-- iter; iter++) { if
(scan(iter,5)) { fprintf(outf,"0xFF.backslash.n");
for (j = 0; j < 8; j++) OutputBit(outfile,1);
 } else { fprintf(outf,"0x00.backslash.n");
for (j = 0; j < 8; j++) OutputBit(outfile,0);
 } } CloseOutputBitFile(outfile);
} else printf ("Can not open output file - %s.backslash.n",
argv[2]); fclose(outf); }
```

```
entity fig25a is Port ( clk_w, reset, wr: in std_logic; add_in :
integer range 0 to 15; data_in : in std_logic_vector(7
downto 0); data_out : out std_logic_vector(7 downto 0);
end fig25a; architecture synth of fig25a is constant depth :
integer := 16; type data_array is array ( integer range <> )
of std_logic_vector (7 downto 0); signal data : data_array
(0 to depth -1); begin process (clk_w) begin if (clk_w='1'
and clk_w'event) then if wr = '0' then data (add_in) <=
data_in; end if; end if; end process; data_out <= data

(add_in); end synth;
```

```
entity fig25b is Port ( clk_w, wr: in std_logic; add_in :
integer range 0 to 15; data_in : in std_logic_vector(7
downto 0); data_out : out std_logic_vector(7 downto 0); end
fig25b; architecture synth of fig25b is constant depth :
integer := 16; constant idepth : integer := (depth - 1); type
data_array is array ( integer range <> ) of std_logic_vector
(7 downto 0); signal data : data_array (0 to depth -1); begin
GEN_LABEL : for I in idepth downto 0 generate data_out
<= DATA(I) when (wr='1' and I=add_in) else (others=>'Z')
Process begin wait until (clk_w'event and clk_w = '1'); if (I =
add_in and wr = '0') then data(I) <= data_in; end if; end
process; end generate GEN_LABEL; end synth;
```

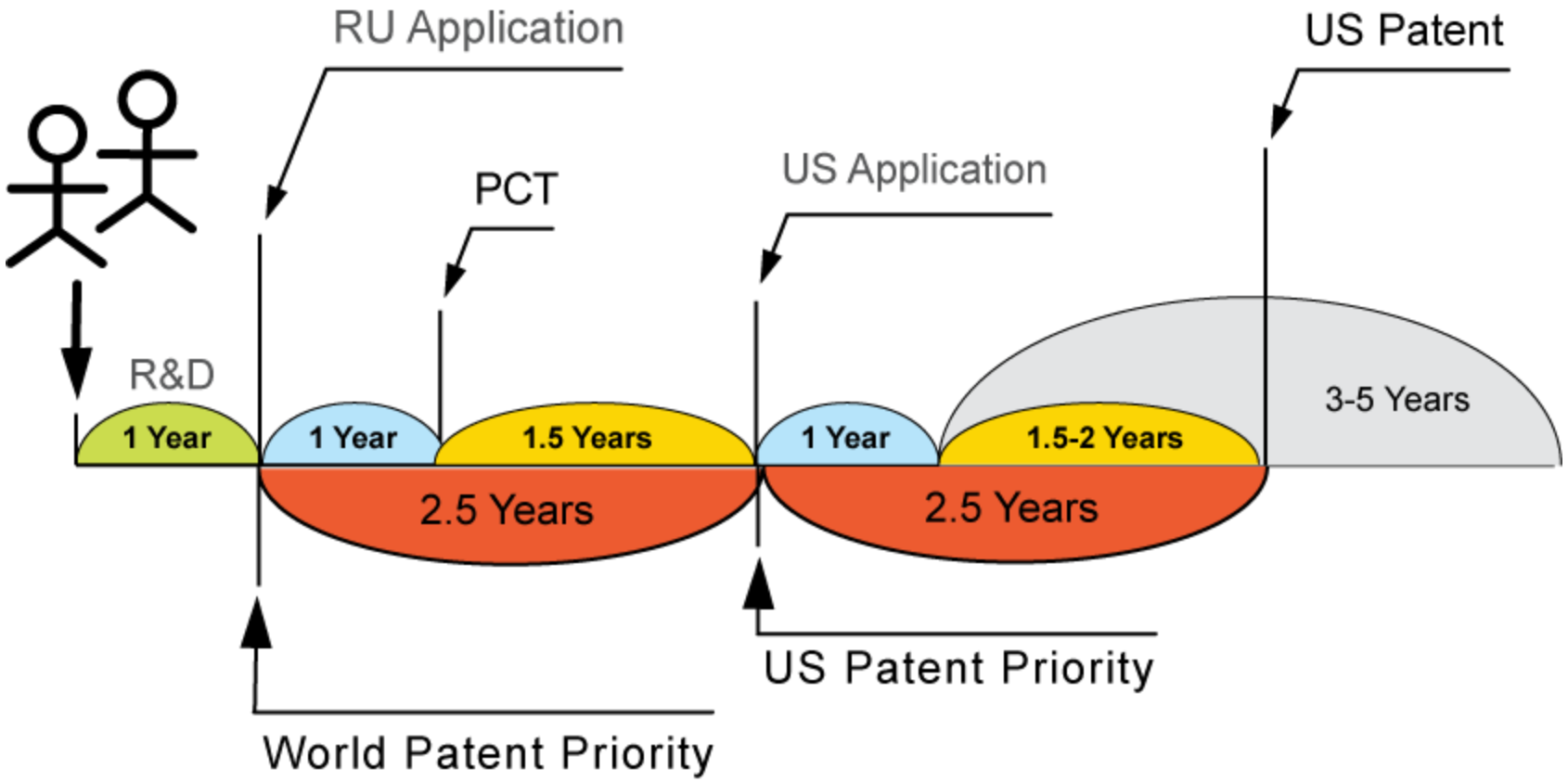
# FPGA


XILINX
VIRTEX-4
XC4VLX200


cc0304
ALTERA
Cyclone TM
EP1C12Q240C8
L BAA9G0313A

# Как это всё реально делается

# USA / 1 патент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US Patent
PCT
US Application
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1 Year
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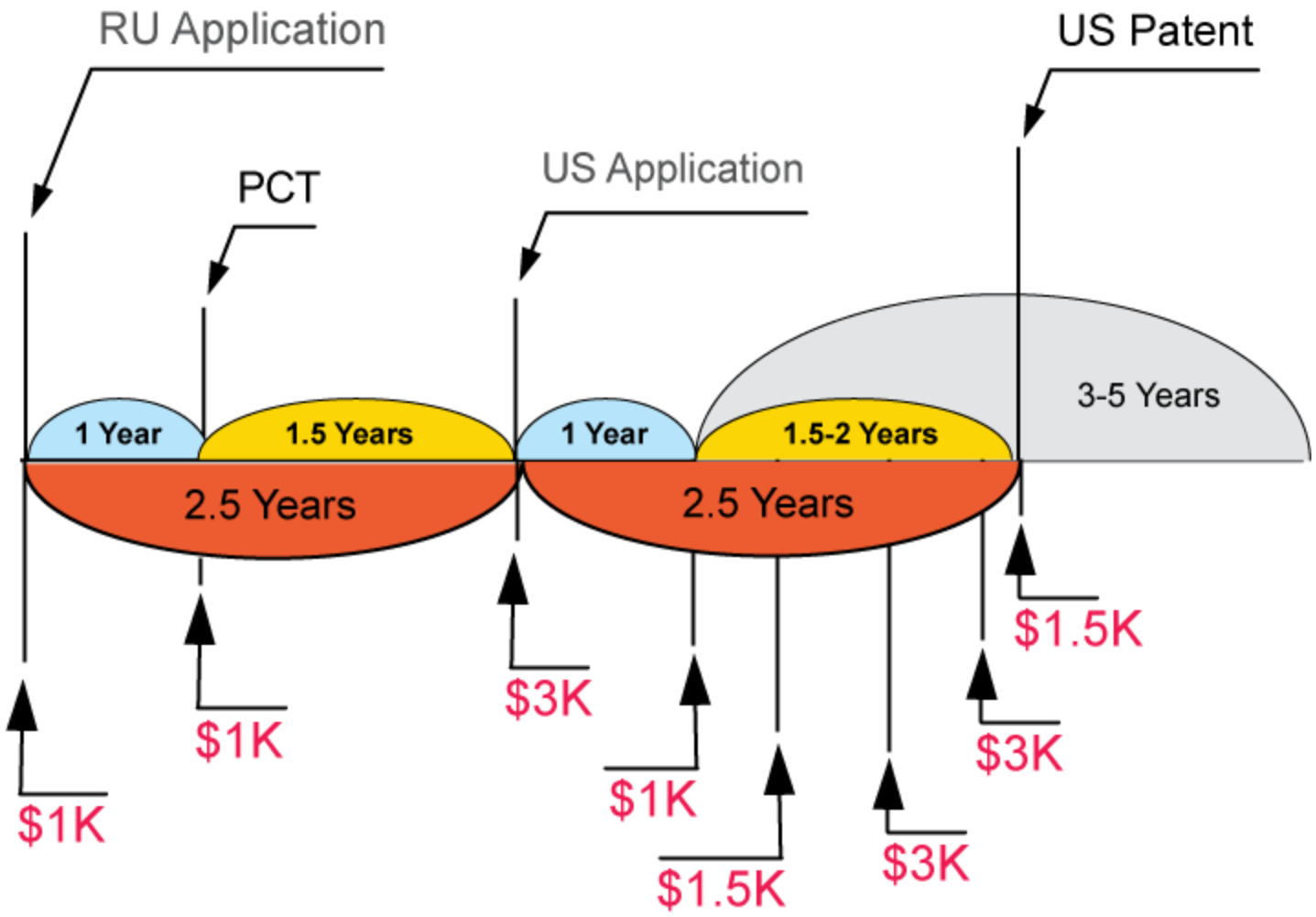
1.5 Years
1 Year
1.5-2 Years
3-5 Years
2.5 Years
2.5 Years
US Patent Priority
World Patent Priority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1 Year
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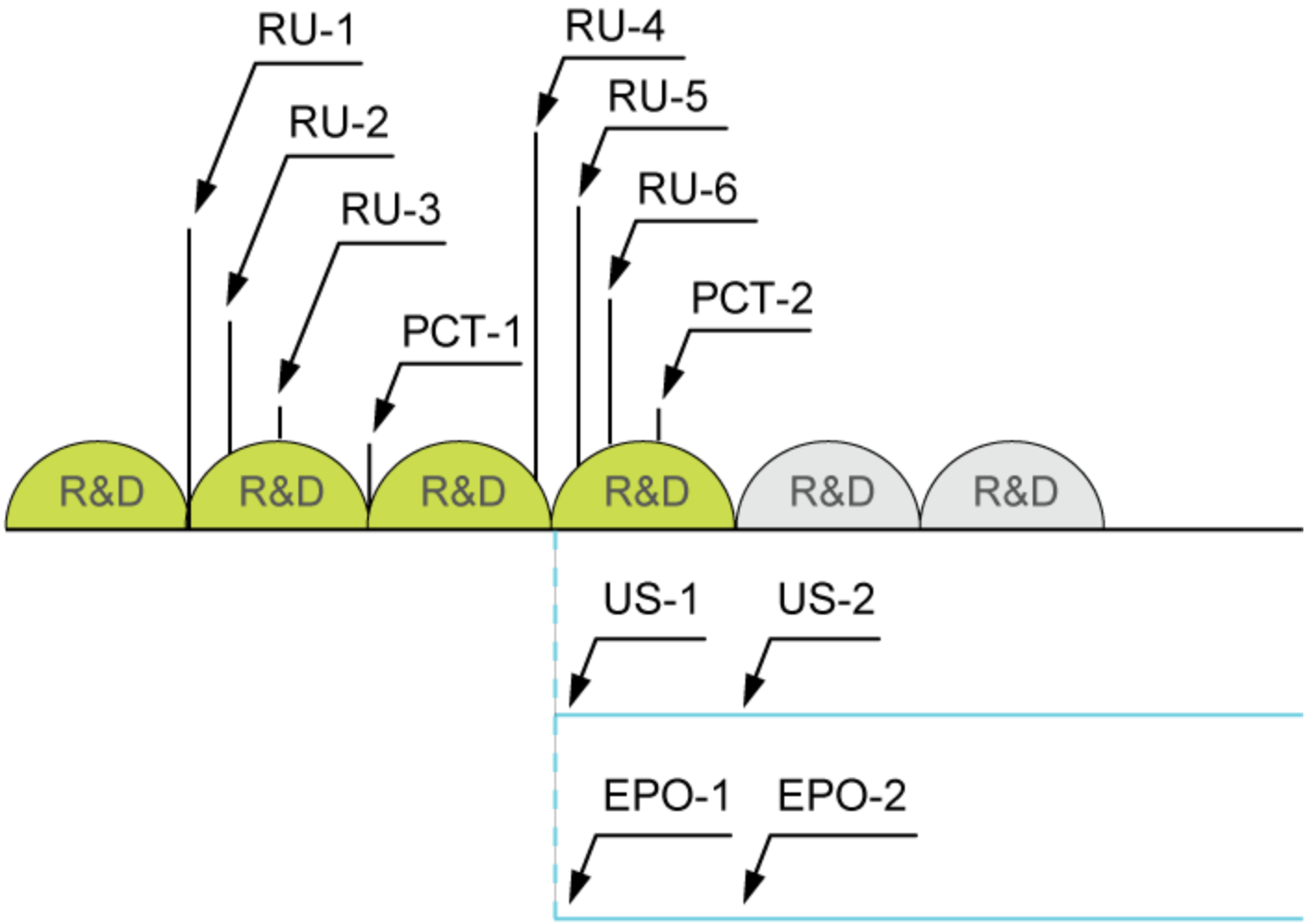
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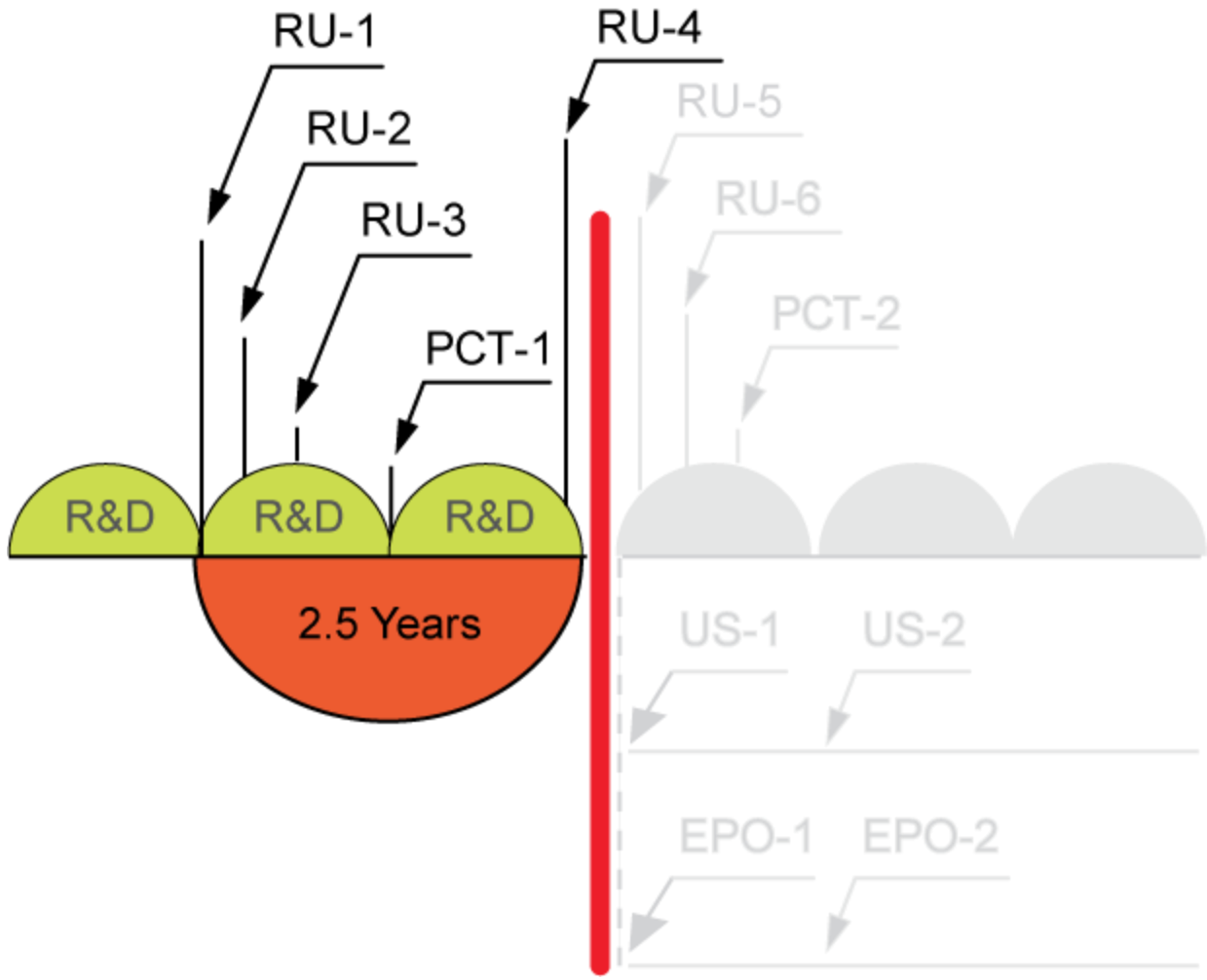
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R&D
R&D
R&D
2.5 Years
US-1
US-2
EPO-1
EPO-2


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