

The World Leader in High Performance Signal Processing Solutions



Blackfin Processor Family & Positioning

Форум DEDF'2009
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Quicklink & Info

Type of Presentation	Details	Audience
Minsk Nov. 2009	Technical, main info, difference	Mixed, 30 min

ESC Key, terminates the Type of Presentation



Roadmap



Go to Selection Table / main DSP groups



Skip to next DSP

In This Presentation:

- The unique architecture of Blackfin[®] explained
- Blackfin family overviews with key/differentiating features and target applications
 - BF512/BF514/BF516/BF518
 - BF522/BF523/BF524/BF525/BF526/BF527
 - BF531/BF532/BF533/BF535
 - BF534/BF536/BF537
 - BF538/BF538F
 - BF542/BF544/BF547/BF548/BF549
 - BF561
- Evaluation and Development with Blackfin Processors
 - Ecosystem
 - Development Tools
 - Design Support and Software Modules

Blackfin Processor

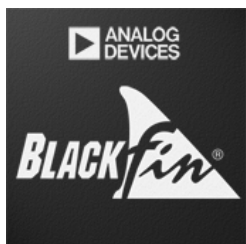
Blackfin 16-/32-bit embedded processors provide software flexibility and scalability for convergent applications:

- Multiformat Audio and Video
- Voice and Image Processing
- Multimode Baseband and Packet Processing
- Control Processing
- Real-Time Security



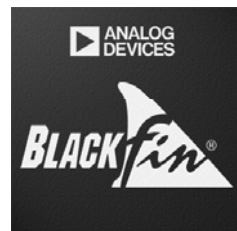
Blackfin Processor—Micro Signal Architecture

The Micro Signal Architecture was crafted with the requirements of a controller, a DSP, and a media processor in mind.



- ... **IS** an architecture that is optimized to perform equally well for signal processing, control processing, and media processing
- ... **CAN** easily be programmed in assembler, C/C++, or mixed
- ... **IS NOT** just a DSP with an enhanced instruction set
- ... **IS NOT** just a processor with a couple of arithmetic units added

Convergent Processing



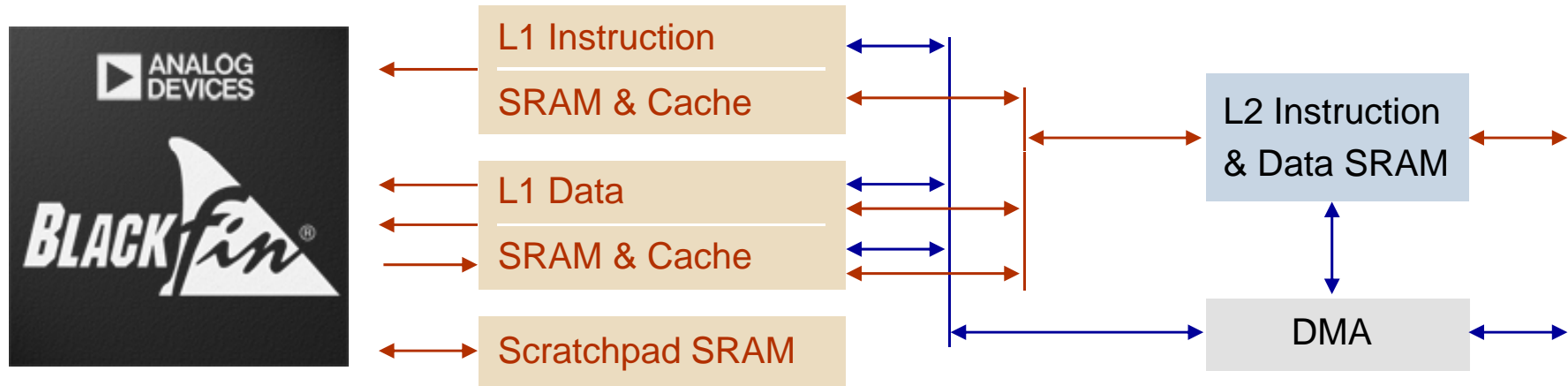
Multimode Connectivity

Embedded Control Processing

Digital Signal Processing



Blackfin Processor—Memory Hierarchy



Hierarchical memory structure

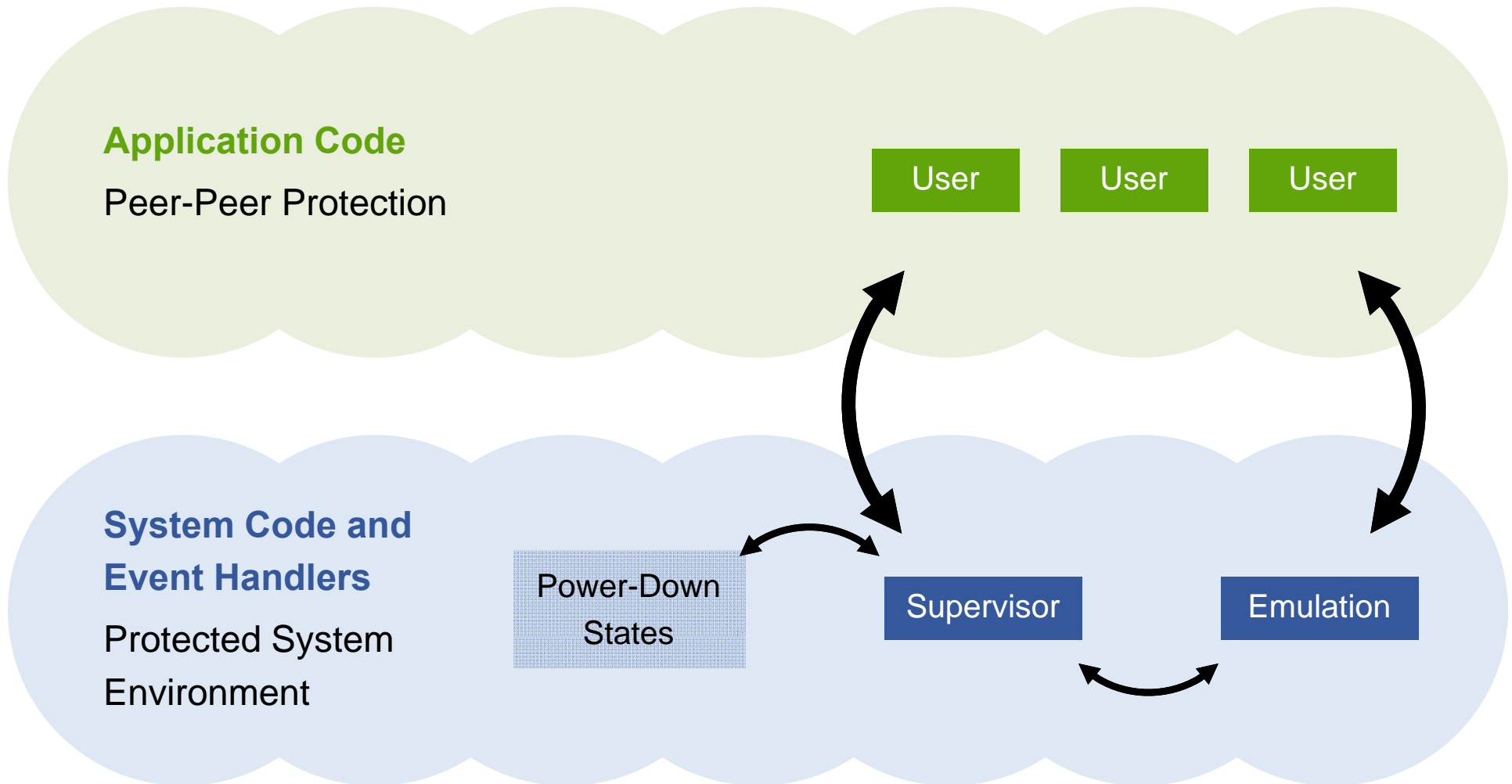
- L2 memory may be on or off chip depending on the specific device

Supports a cache (MCU) and an SRAM (DSP) memory model

- Dynamically configurable between cache and SRAM
- Caches are lockable by way or line
- Cache control instructions: prefetch, flush, and test
- Cache can be configured as write back or write through

Blackfin Processor—MMU Protects You

Supervisor and user protection of memory and registers





Blackfin Processor Core

Blackfin is based on the Micro Signal Architecture jointly developed with Intel® Corporation

Computational units

- Two 40-bit ALUs
- Two 16-bit multipliers
- Four 8-bit video ALUs
- 40-bit shifter

Flexible register file

- Sixteen 16-bit registers for DSP ops
- Eight 32-bit registers for MCU ops

MCU pointers

- 32-bit generic pointers P0–P5
- Stack pointer, frame pointer

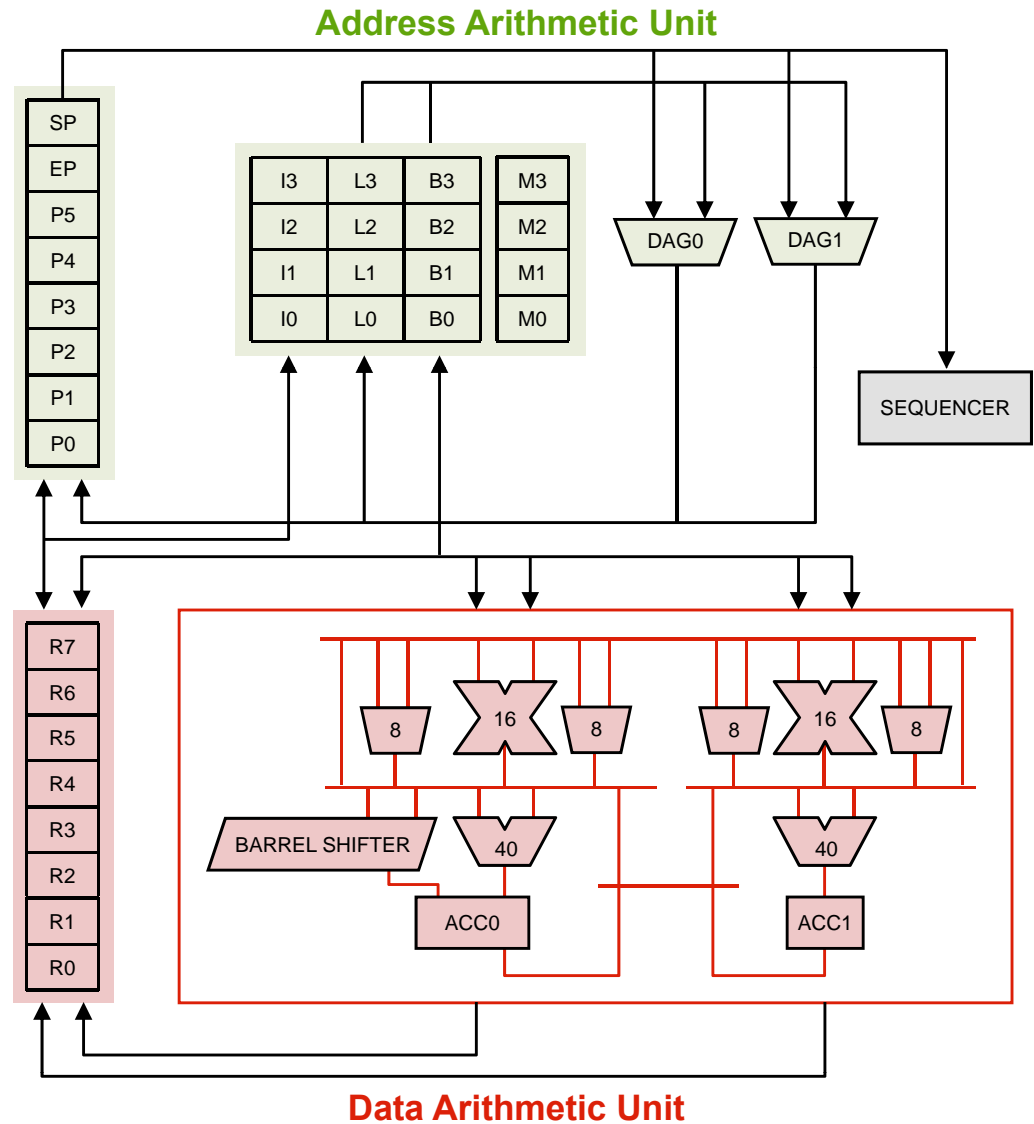
DSP pointers

- Two data address generators
- Four sets of 32-bit registers

Byte addressing by both MCU and DSP pointers

Variable length instructions

- 16-bit instructions for MCU ops
- 32-bit instructions for DSP ops
- Multi-issue, 64-bit instructions





Additional MCU Features in Blackfin

Performance counters

- Two 32-bit counters that count the occurrences of an event
- Provide feedback on the load balancing between resources

Cycle counters

- 64-bit counter, increments on every core clock cycle
- Used to measure the number of core clocks for subroutines

Exception processing as well as interrupt processing

- Exceptions are caused by instructions, such as ...
 - Undefined instruction, illegal instruction, attempted access to a protected memory range
- Interrupts are caused by hardware events

Data packing and unpacking

- DMA channels for SPORTs and PPI allow packing and unpacking
- Instructions to pack and unpack 4 data bytes



Blackfin Peripheral Set (today)

- 10/100 Ethernet MAC
- USB 2.0 OTG High Speed
- CAN[®] 2.0B Controller(s)
- UART(s) and SPORT(s)
- Serial Peripheral Interface (SPI)
- Two Wire Interface (TWI) = I²C
- SDRAM, Flash, DDR, 1.8V mobile DDR, NAND Flash Controller
- 32-bit Watchdog Timer
- Real-time Clock with alarm features
- 32-bit timers and one 32-bit core timer
- PCI 2.2 Master and Slave
- Parallel Peripheral Interface (PPI) and Enhanced PPI (EPPI)
- General Purpose I/Os (Up to 152)
- SD/SDIO Controller
- ATAPI Controller
- Lockbox[™]/OTP Security
- LCD Controller/Overlay Manager
- Keyboard/Rotary Controller



Blackfin Processor Benefits

Reduce BOM by eliminating the need for multiple processors

Blackfin processor combines high performance signal processing (DSP core) and efficient control processing capabilities (RISC functionality).

Flexibly meets needs of the evolving Internet era of signal processing

Optimized for low power processing of audio, video, and communications data.

Extends battery life in portable applications

Software-controlled dynamic power management conserves power.

Easier design with glueless connectivity to popular external devices

Application-tuned system peripherals.

Reduces time to market

Simple, easy to use architecture and tools to speed time to market.

Reduces investment risk through scalability, today and tomorrow

Large portfolio of best-in-class performing processors today with a robust future roadmap.



Blackfin Processor Portfolio

	Future	BF512	BF514 BF516 BF518	BF522 BF524 BF526	BF523 BF525 BF527	BF531 BF532	BF533	BF534 BF536	BF535	BF537	BF538 BF539	BF542 BF544 BF547 BF548 BF549	BF561	Future	
Lowest BOM Cost	●	●		●		●									●
Baseline Connectivity	●	●		●	●	●	●							●	●
System-Level Connectivity			●	●	●			●	●	●	●	●	●		
Low Standby	●	●	●	●											●
Lockbox™ Security		●	●	●	●								●		●
System Integration (Flash, Mixed-Signal)	●	●	●	●	●						●				
600 MHz or Greater					●		●			●			●	●	●
Multicore														●	●

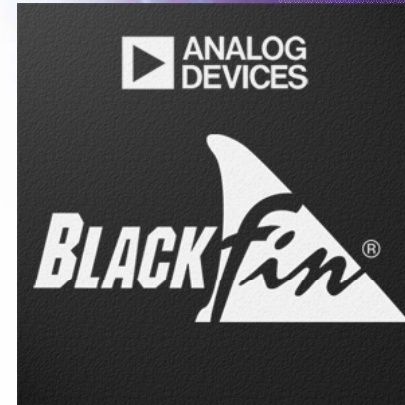
Automotive grade available.



One Processor Is Better Than Two

	Convergent Processor	Heterogeneous Coprocessors
High signal processing performance	●	●
High control processing performance	●	●
Maximum power efficiency	●	
Low latency host-processor communications	●	
Optimized data flow	●	
Most efficient memory utilization	●	
Ideal host for HLL-programmed signal processing	●	
Single tool chain from development to validation	●	
Deterministic task-switching	●	
Single instruction set	●	

The Blackfin BF51x Family



BF51x Block Diagram

Key features of BF51x

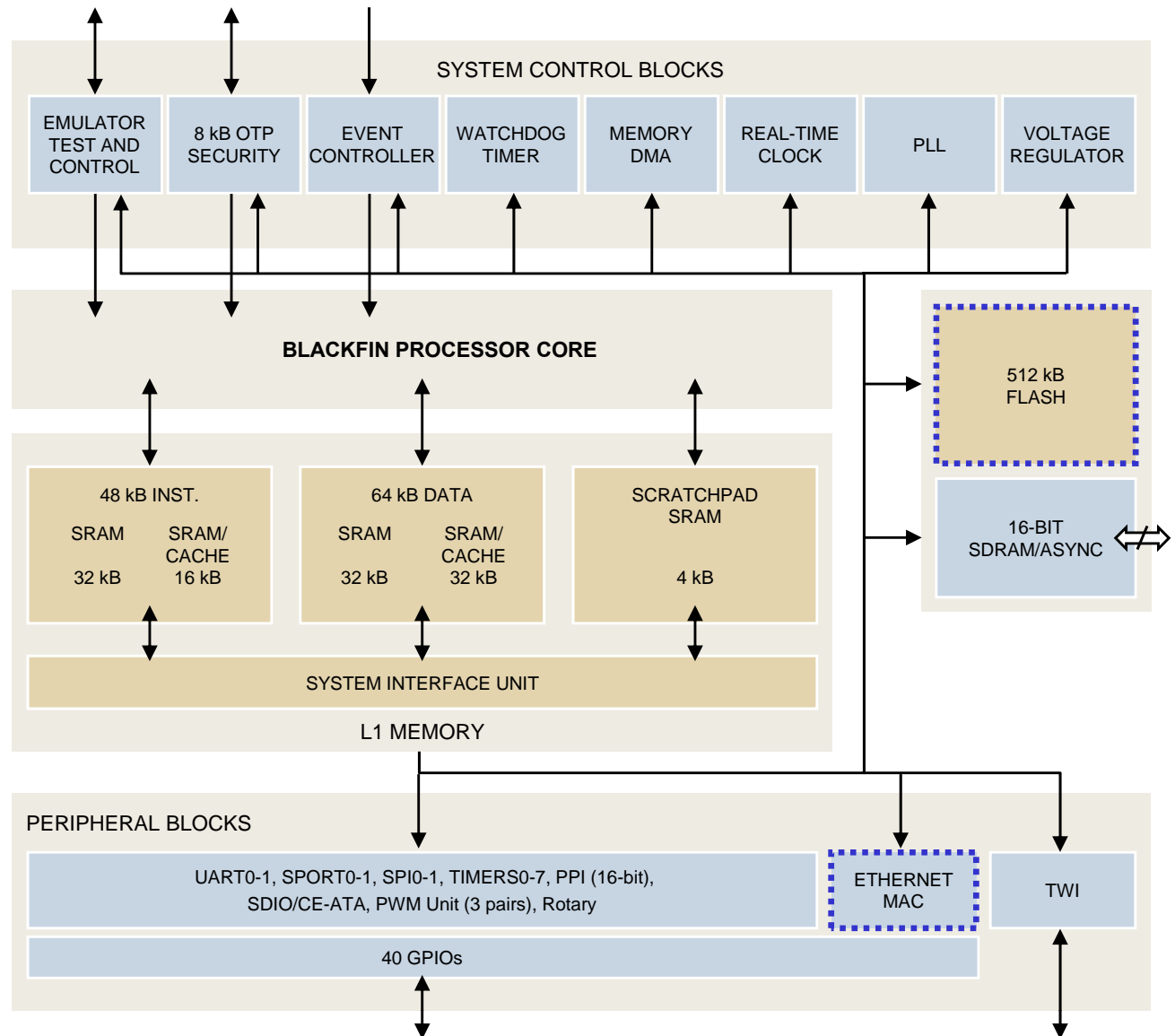
- 400 MHz Blackfin core
- 116 kB L1 on-chip memory
- x1 Ethernet MAC with IEEE-1588
- x1 PPI/LCD controller
- x2 UARTs
- x2 SPORTs
- x2 SPIs
- x1 TWI (I²C)
- x8 timers
- PWM unit with 3 pairs of PWM output
- x1 SDIO/CE-ATA
- x40 GPIOs
- Lockbox/OTP 8 kB
- Rotary
- Optional Flash Memory

Package

- LQFP w/ Exposed Pad
- CSP_BGA

Temperature range

- Industrial



Package and Bond Out Option



Blackfin Feature Comparison

Features	BF512	BF514	BF516	BF518
Ethernet MAC	—	—	Y	Y
IEEE-1588v2 (AVB and I&I)				Y
RSI (MMC, CE-ATA, SDIO)	—	Y	Y	Y
OTP/Security	Y	Y	Y	Y
TWI	1	1	1	1
SPORTs	2	2	2	2
UARTs	2	2	2	2
SPI	2	2	2	2
GP timers	8	8	8	8
Watchdog timers	1	1	1	1
PWM units	Y	Y	Y	Y
RTC	1	1	1	1
Parallel peripheral interface	1	1	1	1
Quadrature encoders	1	1	1	1
GPIOs (muxed)	40	40	40	40
Embedded flash (F versions)—optional	Y	Y	Y	Y
Memory (Bytes)				
L1 instruction SRAM	32 kB	32 kB	32 kB	32 kB
L1 instruction SRAM/cache	16 kB	16 kB	16 kB	16 kB
L1 data SRAM	32 kB	32 kB	32 kB	32 kB
L1 data SRAM/cache	32 kB	32 kB	32 kB	32 kB
L1 scratchpad	4 kB	4 kB	4 kB	4 kB
OTP	8 kB	8 kB	8 kB	8 kB
Boot ROM (not customer configurable)	32 kB	32 kB	32 kB	32 kB
Maximum speed grade	400 MHz	400 MHz	400 MHz	400 MHz
Package options				
176-pin LQFP w/ Exposed Pad 24x24mm	Y	Y	Y	Y
168-ball CSP_BGA 12x12mm	Y	Y	Y	Y

} Areas of differentiation



BF51x Basics

Up to 400 MHz single-core processor; Fully code compatible with BF53x/BF2x

- 16-/32-bit architecture
- Control, signal, and multimedia processing capabilities

Enhanced on-chip memory

- 116 kB L1 memory (48 kB instruction, 64 kB data, 4 kB scratchpad)
- 512 kB SPI flash (BF51xF version)
- Available L3 external 16-bit asynchronous and SDRAM memory access

OTP and Lockbox[®] Secure Technology

Enhanced connections to storage devices and WiFi modules

- 4-/8-bit port SDIO/CE-ATA connectivity: connect SD memory cards and WLAN

Ethernet MAC

- MII and RMII
- IEEE-1588—intended for industrial automation and test and measurement environments

32-bit quadrature counter

- Sense 2-bit quadrature or binary codes emitted by industrial drives



BF51x Basics *(continued)*

Parallel peripheral interface/LCD controller

- Connection to popular video converters and high speed CODECs
- Digital TFT LCD interface with up to 16-bit display capability

Enhanced serial connections

- Up to 2xSPORT, 2xUART, 1xTWI, 2xSPI

x8 32-bit timers for PWM, input capture, event counter

PWM unit

- Three pairs of PWM output

Up to 40 GPIOs

Watchdog timer

- 32-bit timer to implement a software watchdog function

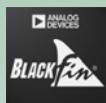
Operating temperature -40°C to +85°C

Blackfin BF51x Market-Specific Features

“Enhanced” VoIP



Blackfin enables better quality and more features for the same price



Blackfin
BF516

Key features:

- Includes 10/100 eMAC for low BOM cost
- Availability of GPS VE
- SDIO for WiFi
- 400 MHz allows addition of several channels and features like fax over IP
- Reference platform available on μ Clinux™

Portable



Blackfin delivers ultra-low power processing in conjunction with connectivity to low power devices



Blackfin
BF512
BF514

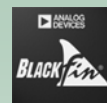
Key features:

- Low power—8.5 mW
- Includes removable storage interfaces (WiFi, SD cards, CE-ATA devices)
- Includes CE-ATA and eMMC

Industrial & Instrumentation



Blackfin enables smart industrial equipment



Blackfin
BF512
BF518

Key features:

- IEEE 1588 eMAC for precision time syncing over Ethernet
- Low power for portable applications
- PWM output for 3-phase inductor applications
- LQFP package

Automotive



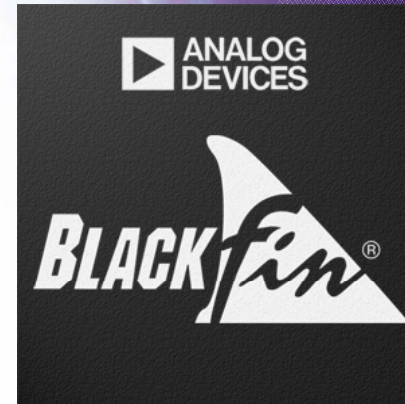
Blackfin enables CE connectivity within the car



Key features:

- 400 MHz at a low BOM

The Blackfin BF52x Family





The Blackfin BF52x Family of Processors

- The BF52x family is taking portable consumer devices to the next level of application features and services
- Enabling more features while increasing battery life
- New software and tools for converged applications

Portable media player

- WiFi networking
- Content protection
- eCommerce
- Lockbox Secure Technology

Internet telephony

- VoIP stack
- IP phone
- Analog telephone adapters (ATA)

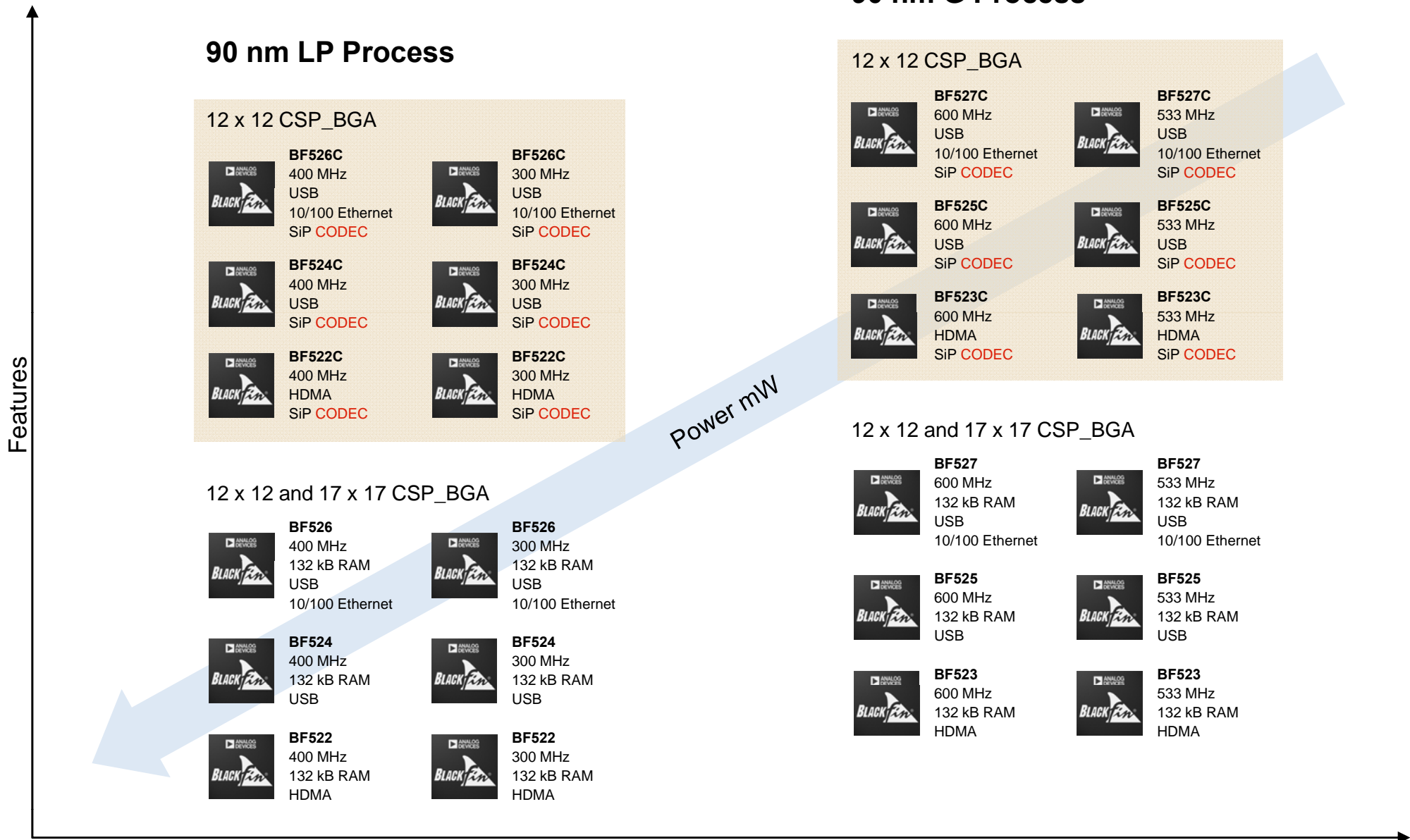
IP cameras

- Video CODECs
- Video doorbell

Mobile radio/TV

- T-DMB/DAB-IP
- DAB/Digital Radio Mondiale
- IP broadcast

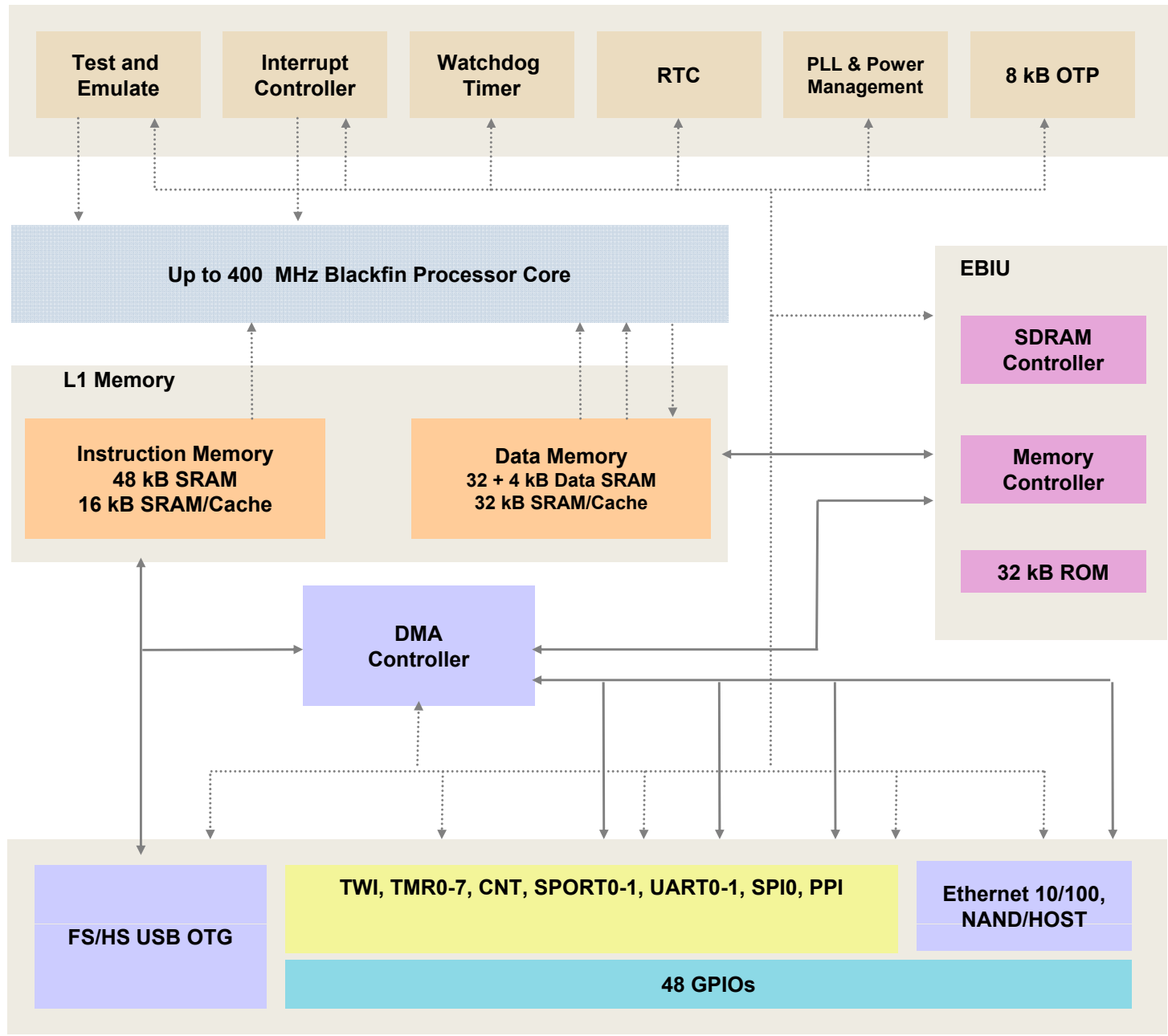
BF52x Portfolio





BF522...BF527

Differentiation:
HOST
USB
ETHERNET





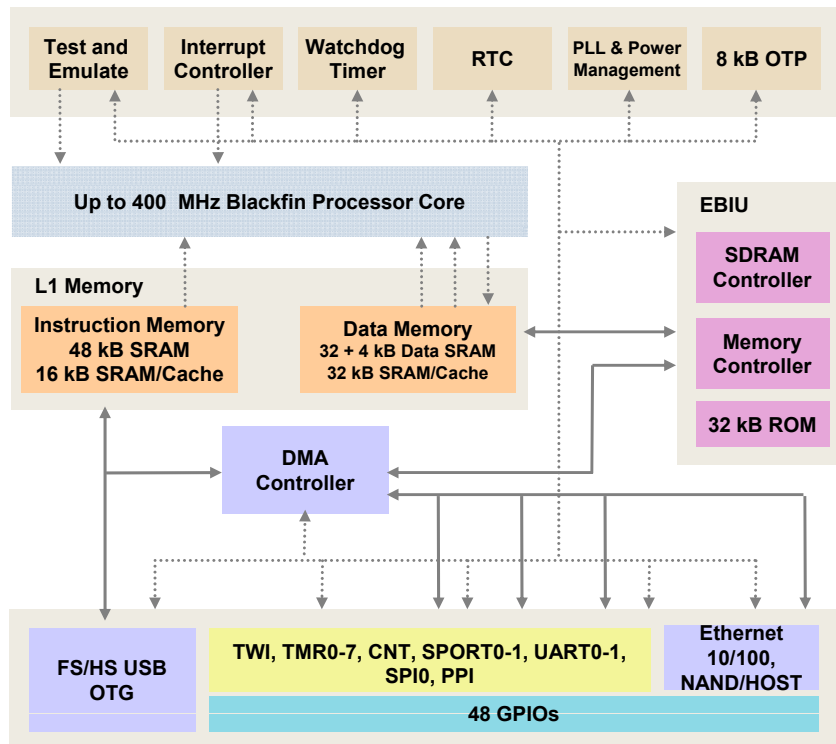
BF522/BF524/BF526—400 MHz

Ultra-low power embedded processor

BF52x 400 MHz family

- Flexible peripheral options
- Low static current

Fully software compatible with existing BF536, BF532/1



Performance	Up to 400 MHz 16-/32-bit core (1.8 GB/s bandwidth)						
Power consumption	<table border="0"> <tr> <td>Hibernate</td> <td>50 uA</td> </tr> <tr> <td>Deep sleep (1.0 V) @ 1.0 V, 100 MHz</td> <td>2 mA @ +25°C, 6 mA @ +85°C 20 mA @ +85°C, 24 mA @ +85°C</td> </tr> <tr> <td>@1.25 V, 350 MHz</td> <td>99 mA @ +25°C, 106 mA @ +85°C</td> </tr> </table>	Hibernate	50 uA	Deep sleep (1.0 V) @ 1.0 V, 100 MHz	2 mA @ +25°C, 6 mA @ +85°C 20 mA @ +85°C, 24 mA @ +85°C	@1.25 V, 350 MHz	99 mA @ +25°C, 106 mA @ +85°C
Hibernate	50 uA						
Deep sleep (1.0 V) @ 1.0 V, 100 MHz	2 mA @ +25°C, 6 mA @ +85°C 20 mA @ +85°C, 24 mA @ +85°C						
@1.25 V, 350 MHz	99 mA @ +25°C, 106 mA @ +85°C						
Address range	up to 512 MB						
On-chip memory	132 kB SRAM 8 kB OTP memory						
New peripherals/features	<ul style="list-style-type: none"> • FS/HS USB OTG • 10/100 Ethernet MAC • NAND flash interface • TWI (I²C) • PPI • SPI • 2 x SPORT • 2 x UART • 48 GPIOs • Code security 						
Bandwidth	<ul style="list-style-type: none"> • 266 Mbps I/O • 266 Mbps DMA • 266 Mbps memory DMA 						
Voltage	1.0 V to 1.2 V (INT) 1.8 V to 3.3 V (EXT)						
Temperature range	<ul style="list-style-type: none"> • 0°C to +70°C ambient • -40°C to +85°C ambient 						
Package	<ul style="list-style-type: none"> • 289 CSP_BGA 12 x 12 (0°C to +70°C) • 208 CSP_BGA 17 x 17 (-40°C to +85°C) 						



BF523/BF525/BF527—Up to 600 MHz

Low power embedded processor

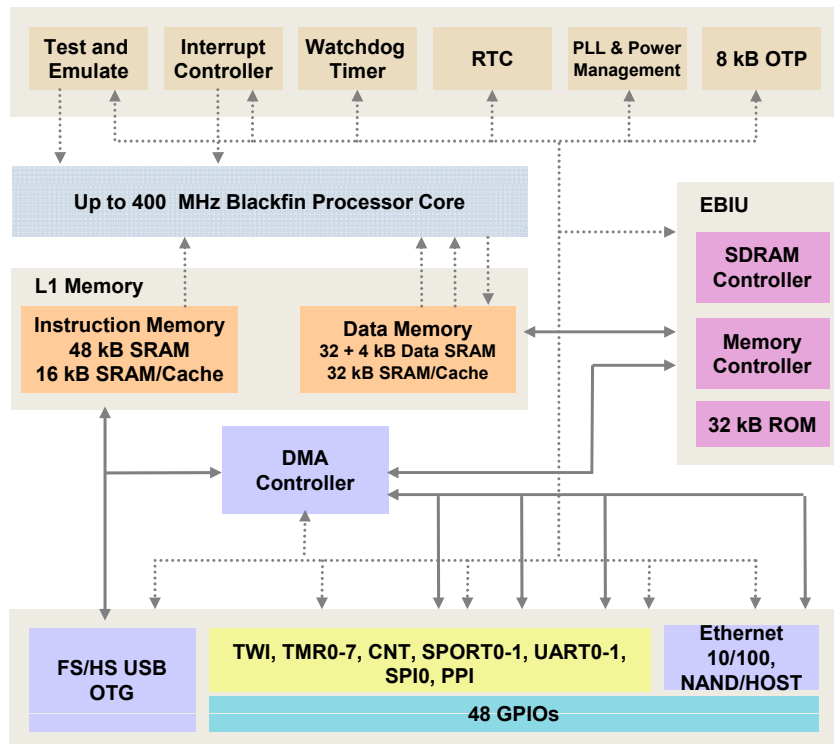
BF52x family up to 600 MHz

MIPS/\$ leadership

Flexible peripheral options

Low dynamic power

Fully software compatible with existing BF53x family



Performance	Up to 600 MHz 16-/32-bit core (2.4 GB/s bandwidth)								
Power consumption	<table border="1"> <tr> <td>Deep sleep (1.0 V)</td> <td>10 mW</td> </tr> <tr> <td>@ 1.0 V, 300 MHz</td> <td>82 mW</td> </tr> <tr> <td>@ 1.0 V, 400 MHz</td> <td>99 mW</td> </tr> <tr> <td>@ 1.2 V, 600 MHz</td> <td>216 mW</td> </tr> </table>	Deep sleep (1.0 V)	10 mW	@ 1.0 V, 300 MHz	82 mW	@ 1.0 V, 400 MHz	99 mW	@ 1.2 V, 600 MHz	216 mW
Deep sleep (1.0 V)	10 mW								
@ 1.0 V, 300 MHz	82 mW								
@ 1.0 V, 400 MHz	99 mW								
@ 1.2 V, 600 MHz	216 mW								
SDRAM Address range	up to 512 MB								
On-chip memory	132 kB SRAM 8 kB OTP memory								
New peripherals/features	<ul style="list-style-type: none"> • HS USB OTG • 10/100 Ethernet MAC • NAND flash interface • Host interface • TWI (I²C) • PPI • SPI • 2 x SPORT • Extended GPIO • Code security (OTP) 								
Bandwidth	<ul style="list-style-type: none"> • 266 Mbps I/O • 266 Mbps DMA • 266 Mbps memory DMA 								
Voltage	0.95 V to 1.2 V (INT) 1.8 V to 3.3 V (EXT)								
Temperature range	<ul style="list-style-type: none"> • -40°C to +85°C ambient • 0°C to +70°C ambient 								
Package	<ul style="list-style-type: none"> • 289 CSP_BGA 12 x 12 (0°C to +70°C) • 208 CSP_BGA 17 x 17 (-40°C to +85°C) 								

BF523/BF525/BF527 Product Comparison

	BF523	BF525	BF527
Feature			
HDMA	Y	Y	Y
USB	-	Y	Y
Ethernet MAC	-	-	Y
TWI	1	1	1
SPORTs	2	2	2
UARTs	2	2	2
SPI	1	1	1
GP timers	8	8	8
Watchdog timers	1	1	1
NAND flash	Y	Y	Y
RTC	1	1	1
Parallel peripheral interface	1	1	1
GPIOs	48	48	48
Embedded CODEC (-C versions)	Y	Y	Y
Memory (bytes)			
L1 instruction SRAM	48 kB	48 kB	48 kB
L1 instruction SRAM/cache	16 kB	16 kB	16 kB
L1 data SRAM	32 kB	32 kB	32 kB
L1 data SRAM/cache	32 kB	32 kB	32 kB
L1 scratchpad	4 kB	4 kB	4 kB
OTP	8 kB	8 kB	8 kB
Boot ROM (not customer configurable)	32 kB	32 kB	32 kB
Maximum speed grade	600 MHz	600 MHz	600 MHz
Package options			
208-ball CSP_BGA 17 x 17 0.8 mm	Y	Y	Y
289-ball CSP_BGA 12 x 12 0.5 mm	Y	Y	Y

} Differentiation





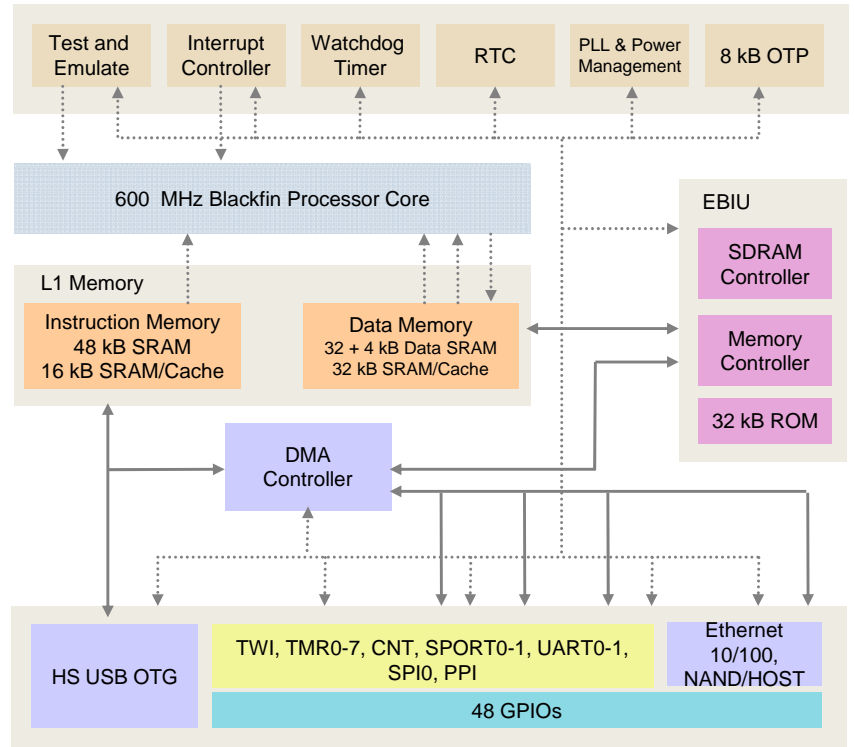
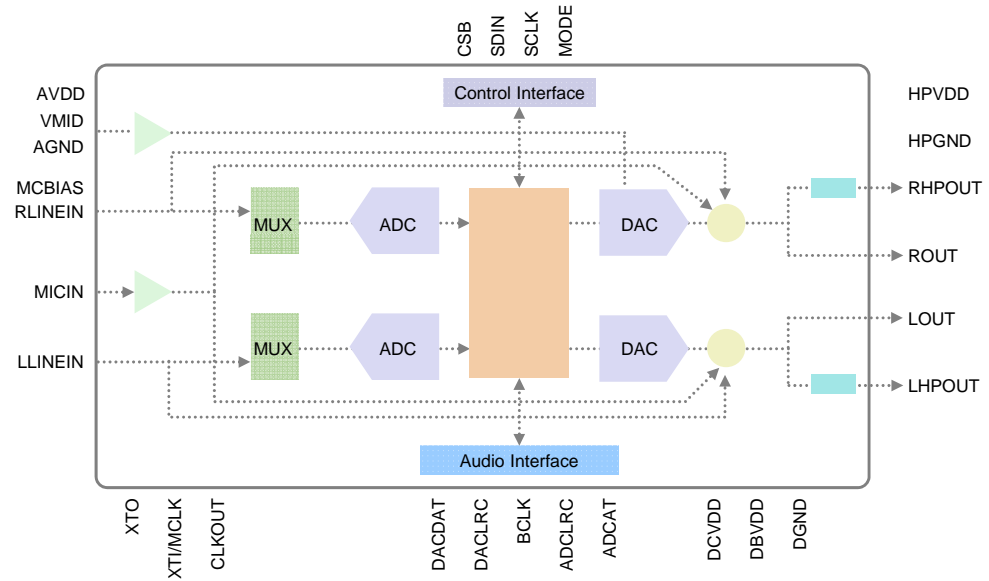
Embedded Audio CODEC

BF52xC

- HS USB OTG/NAND Interface
- Embedded low power CODEC supports a System in Package (SiP)
- Versions available with 300 through 600 MHz BF52x

CODEC

- The BF52xC supports a SiP implementation of a low power stereo CODEC with integrated headphone driver
- The CODEC is designed specifically for low power applications, including MP3 audio and speech players and recorders
- Further information on the CODEC specification and features can be provided under NDA



BF522/BF524/BF526 Product Comparison

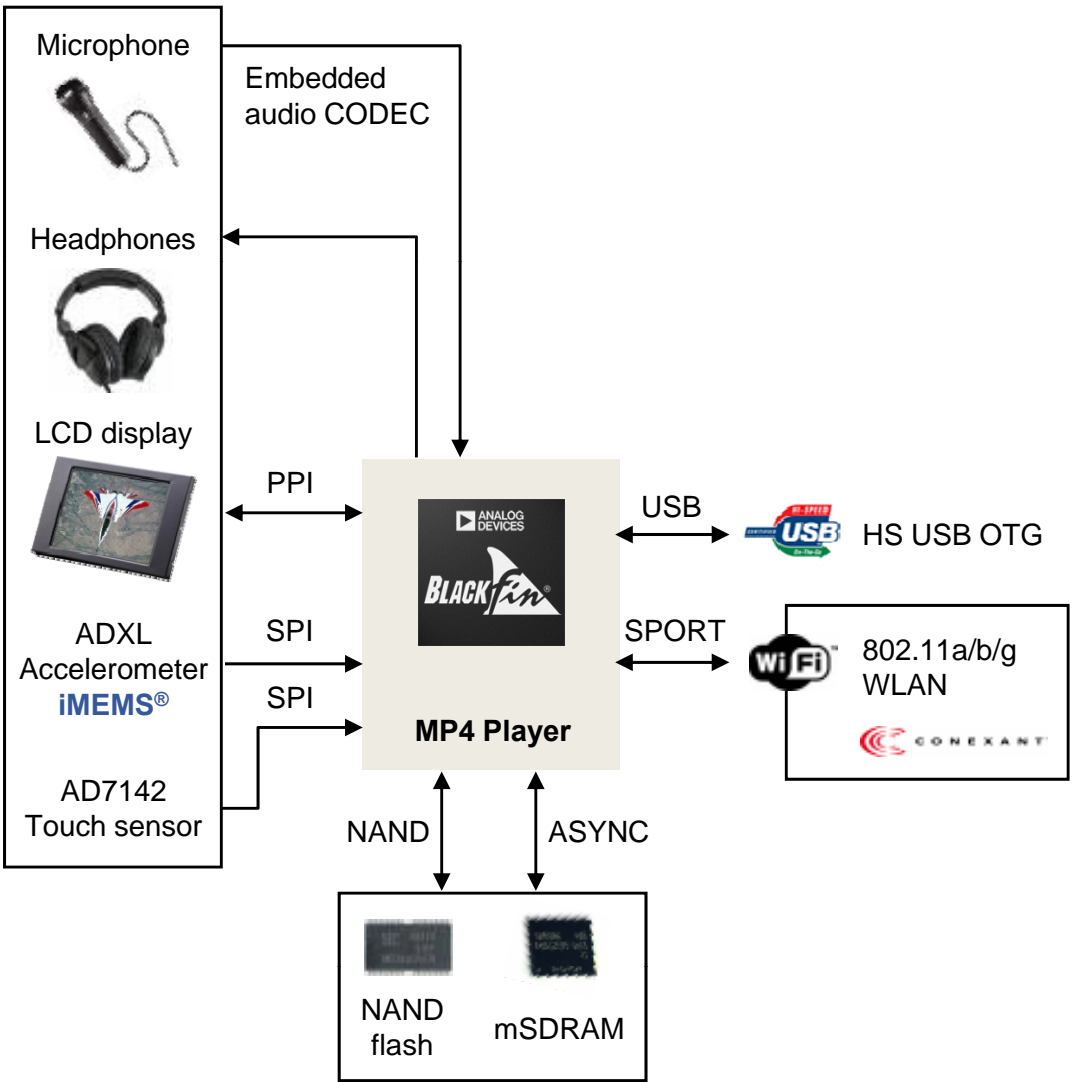
	BF522	BF524	BF526	
Feature				
HDMA	Y	Y	Y	} Differentiation
USB	-	Y	Y	
Ethernet MAC	-	-	Y	
TWI	1	1	1	
SPORTs	2	2	2	
UARTs	2	2	2	
SPI	1	1	1	
GP timers	8	8	8	
Watchdog timers	1	1	1	
NAND flash	Y	Y	Y	
RTC	1	1	1	
Parallel peripheral interface	1	1	1	
GPIOs	48	48	48	
Embedded CODEC (-C versions)	Y	Y	Y	
Memory (bytes)				
L1 instruction SRAM	48 kB	48 kB	48 kB	
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L1 data SRAM	32 kB	32 kB	32 kB	
L1 data SRAM/cache	32 kB	32 kB	32 kB	
L1 scratchpad	4 kB	4 kB	4 kB	
OTP	8 kB	8 kB	8 kB	
Boot ROM (not customer configurable)	32 kB	32 kB	32 kB	
Maximum speed grade	400 MHz	400 MHz	400 MHz	
Package options				
208-ball CSP_BGA 17 x 17 0.8 mm	Y	Y	Y	
289-ball CSP_BGA 12 x 12 0.5 mm	Y	Y	Y	





Connectivity Everywhere—Portable Media Player

Audio playback of WMA9 from MLC NAND flash w/WMDRM-PD 33.9 (500 mAhr) battery hours

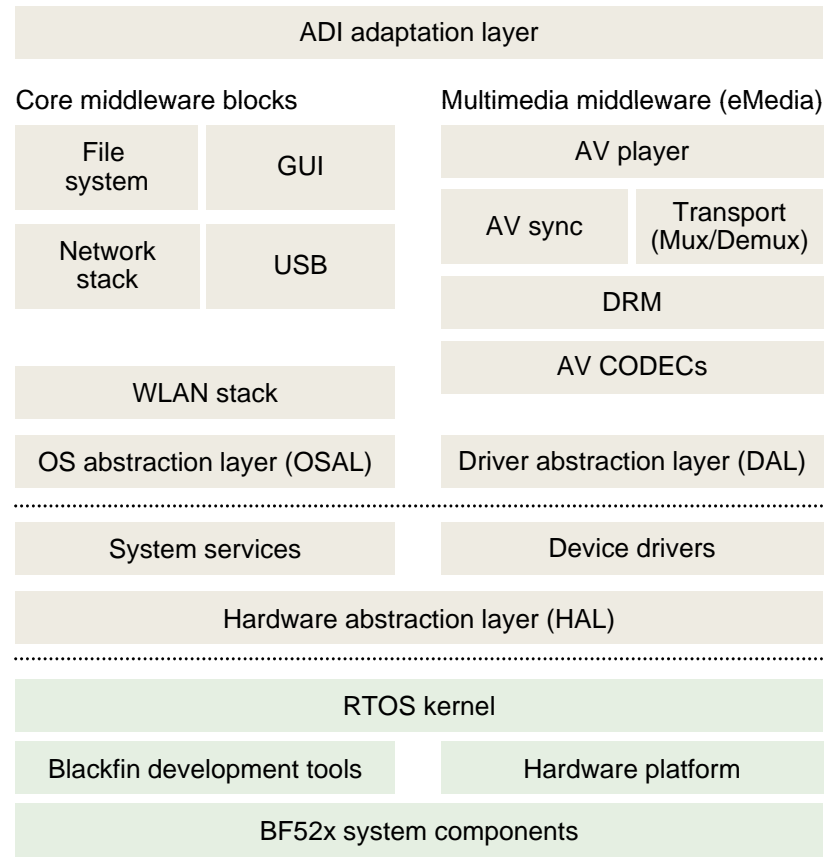


Platform software

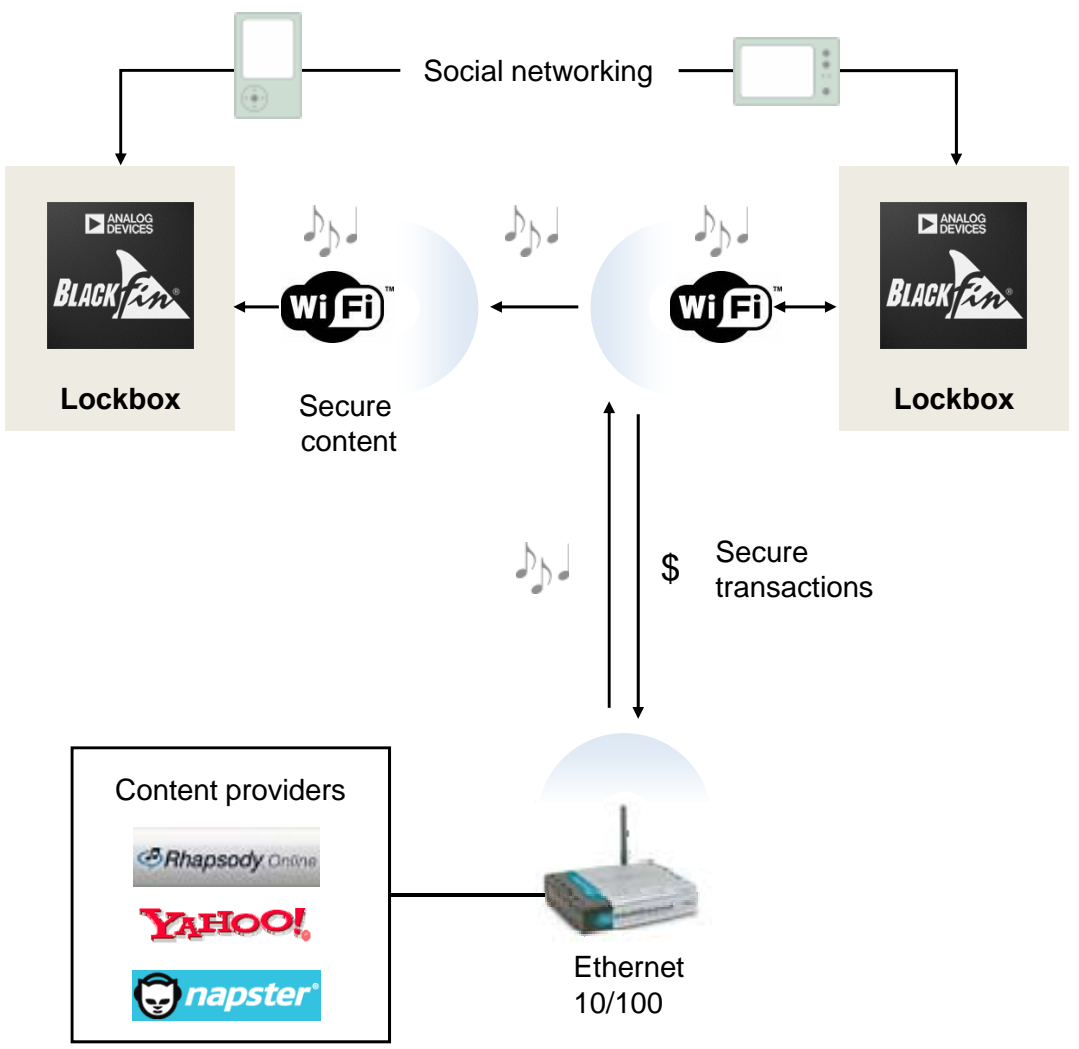
Applications



Middleware layer



eCommerce/Content Protection



Lockbox Secure Technology for Blackfin

Benefits:

IP protection

- Ensure code has not been altered and comes from the appropriate source through authentication
- Verify a code or data image against its embedded digital signature

Prevention of mass copying

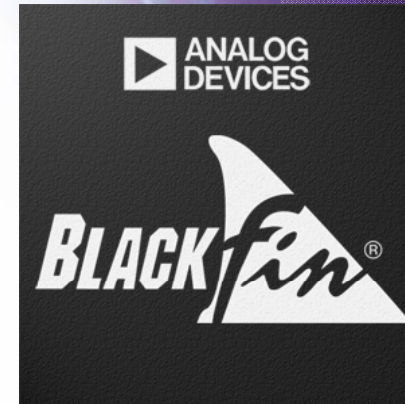
- Utilize unique chip ID to “lock” processor to one specific boot source/device
- Identify valid media content—digital rights management

Secure transactions

- Support cryptographic encryption/decryption when confidentiality is required



The Blackfin BF542/BF544/BF547/ BF548/BF549 Family



Blackfin BF542/BF544/BF547/BF548/BF549

Deliver high system performance for convergent applications

- Increased I/O bandwidth (2x)
- Increased on-chip memory
- Rich peripheral set

Embedded with new Lockbox Secure Technology

Meet the challenges of designing electronics for today's convergent applications and beyond

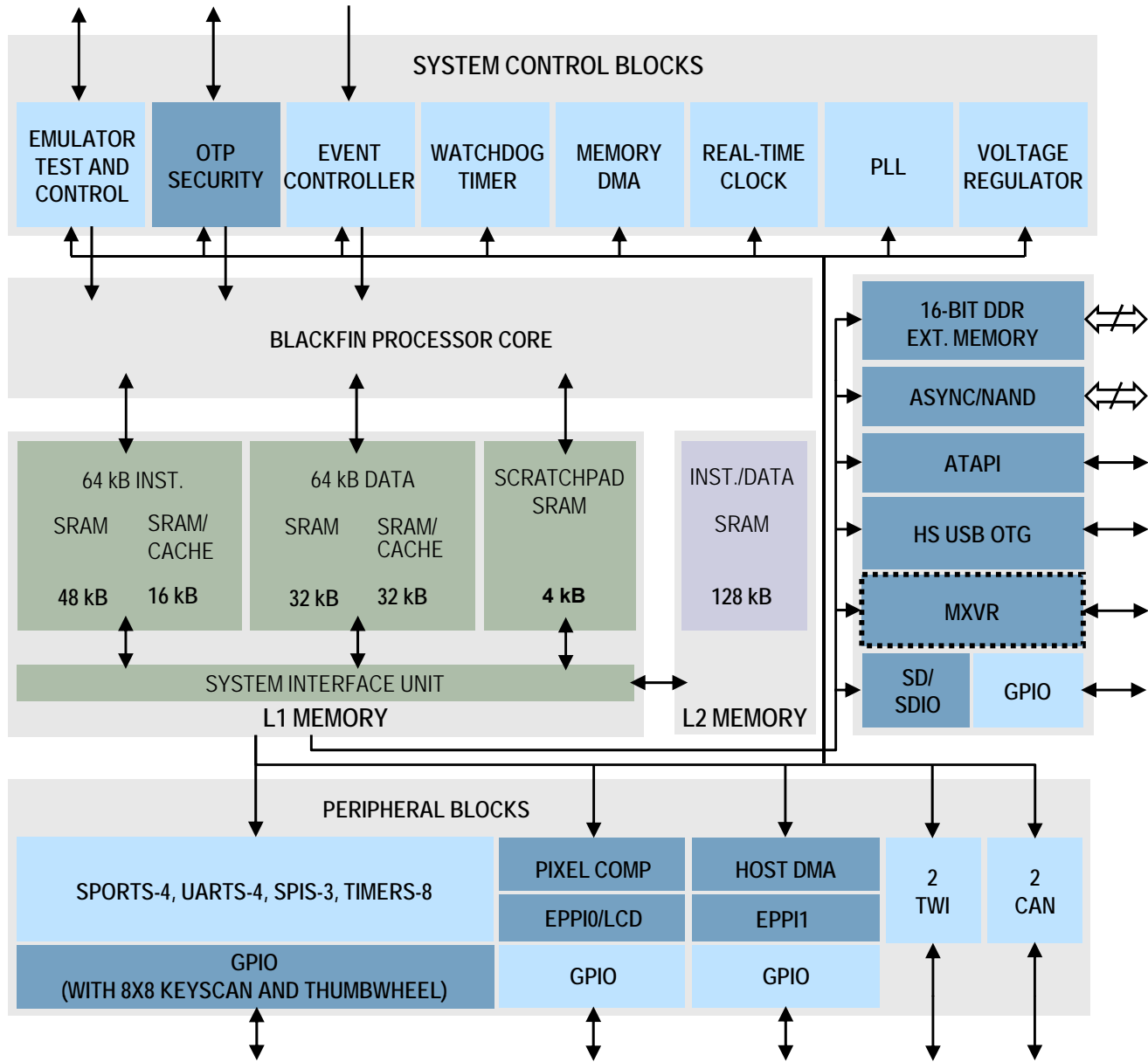
Target Convergent Applications:



- Avionics communications
- Industrial control and factory automation
- Wireless telecommunications, radios, and equipment
- Digital radio
- Security and access control systems
- Audio jukebox
- Navigation
- Handsfree phone operation



BF547/BF548/BF549 Block Diagram



Applicable markets:

- Advanced vehicle infotainment
- Mobile communications
- Security and access control systems
- Industrial control and factory automation
- Portable media players

Core frequency:

- Up to 600 MHz

Memory:

- 260 kB on-chip L1 and L2

Package:

- 400-ball, 17 mm x 17 mm CSP_BGA, 0.8 mm pitch
- -40°C/+85°C ambient

- Existing Blackfin Peripheral
- New Blackfin Peripheral
- MXVR- BF549 Only





BF54x Family Basics

Up to 600 MHz single core processor; fully code compatible with BF53x

Enhanced Memory Interfaces

- DDR1 memory support
 - Optional products available with 1.8V mobile DDR support
- NAND, NOR, CF: supporting cost-effective storage
- ATAPI interface: audio and video ripping to HDD, DVD

Lockbox Secure Technology

Enhanced connections to storage devices

- HS USB OTG: connectivity to portable storage media and devices
- SDIO connectivity: connect to WLAN or BT

Enhanced and multiple PPIs

- Connection to popular video converters and high speed CODECs
- Digital TFT LCD interface with up to 24-bit display capability

Pixel compositor

- Hardware accelerator for color conversion, alpha blending, and overlays for MIPS reduction

Enhanced serial connections

- Up to 4xSPORT, 4xUART, 2xTWI, 3xSPI, 2xCAN
- 1xup/down counter, 8 x 8 keyscan/keyboard interface



BF54x Family Memory

On-chip

- 132 kB L1 memory (64 kB instruction, 64 kB data, 4 kB scratchpad)
 - Equivalent to the BF534/BF537 devices
- Up to 128 kB L2 unified instruction/data SRAM depending on version
- OTP secure locations

Off-chip

- 16-bit asynchronous memory interface
 - 4 X 64 MB NOR linear addressing
 - Direct NAND addressing
 - Burst-mode NOR capability
- Separate synchronous memory interface
 - 512 MB DDR1 memory
 - 1.8 V mobile DDR memory

BF54x Family Peripherals

Parallel ATAPI-6 interface

- Separate interface from DDR memory subsystem for access to HDD, DVD, etc.
- Supports max DVD transfer rates
- Multiplexed with asynchronous memory interface

High speed USB OTG interface with integrated PHY

Enhanced PPIs

- Up to 75 MHz operation, for connection to high speed ADCs and DACs
- EPPI0 can connect to 18-bit and 24-bit RGB LCD displays
- EPPI1 can be split into two independent 8-bit EPPIs (EPPI1/EPPI2)
- EPPI clock sourced internally or externally

Pixel compositor offloads compute-intensive video and imaging tasks

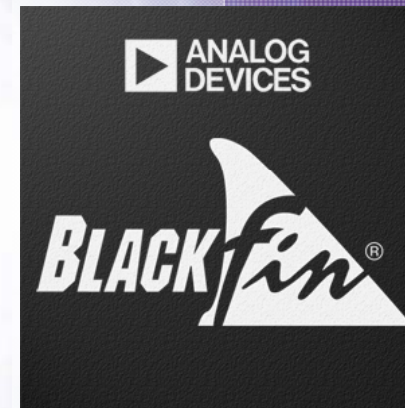
- RGB<->YUV color conversion
- Graphics blending
- Image and video overlays

Secure digital host

- 4-bit port for connection to SD memory cards and SDIO modules like WLAN and Bluetooth®

Evaluation and Development with Blackfin Processors

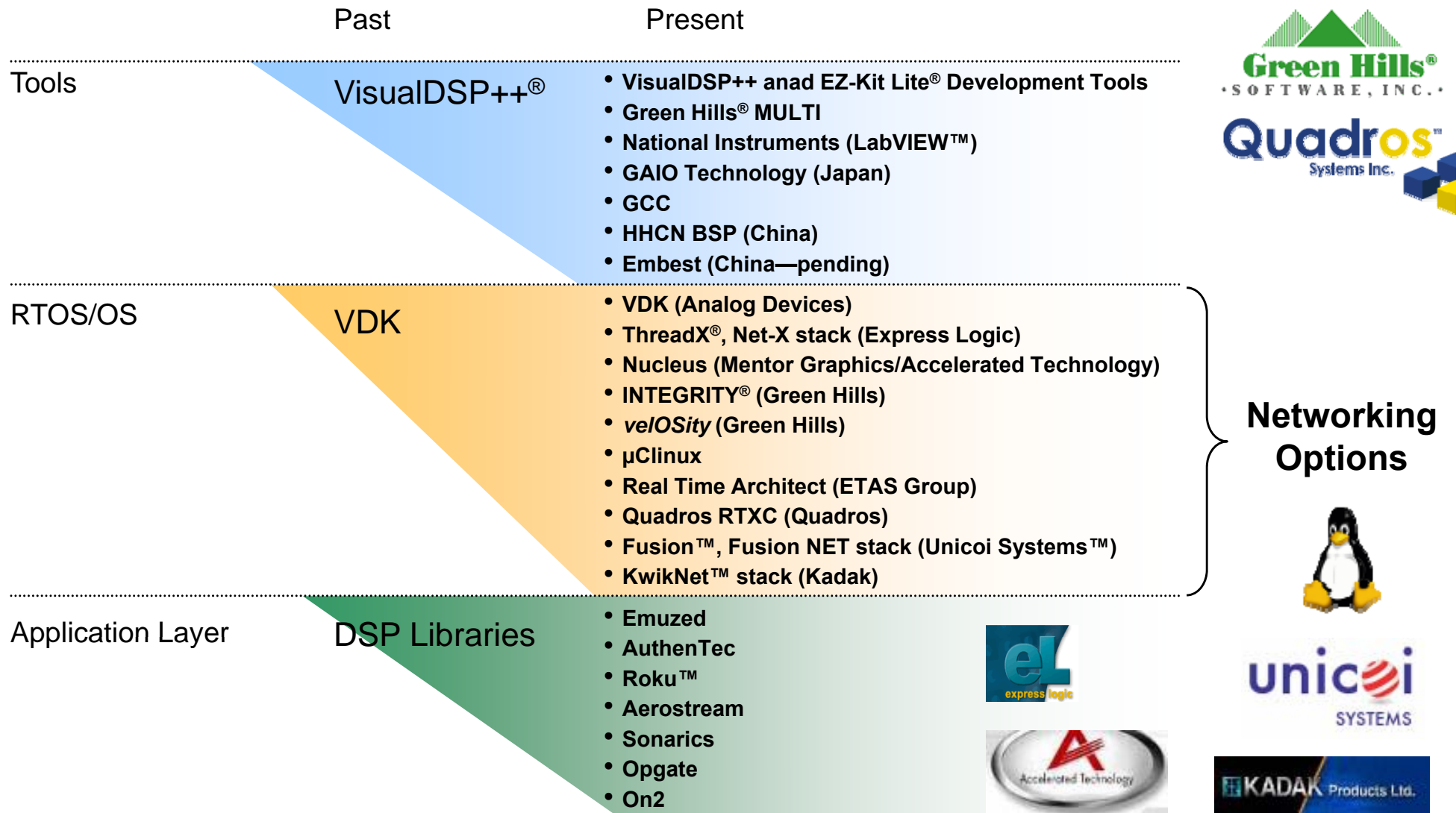
- Ecosystem
- Development Tools
- Design Support & Software Modules





The Blackfin Ecosystem

Tools, RTOS and network stacks/graphics, etc.*





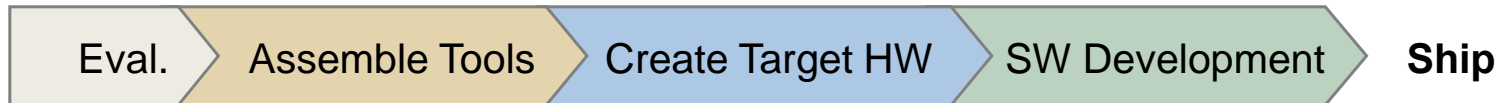
Open-Source Linux Tool Chain

www.blackfin.uclinux.org

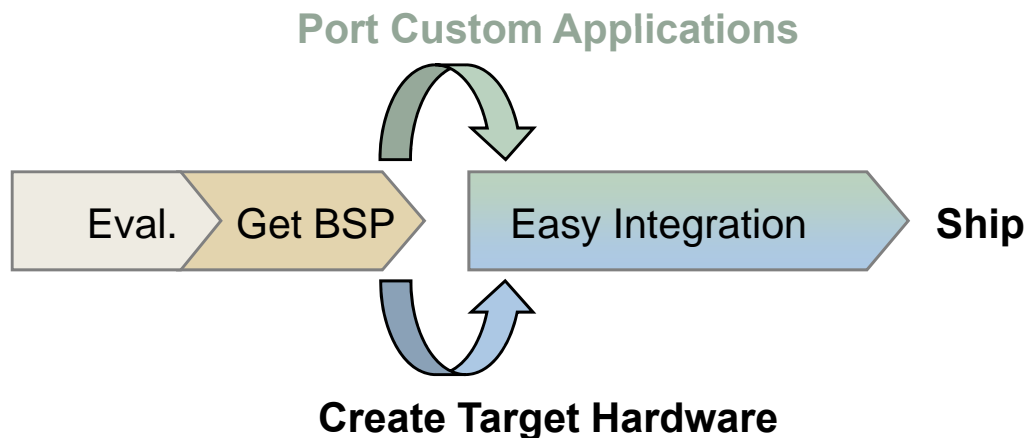
- Grass-roots Blackfin developer program
- ADI's tools infrastructure investment
Seeds the open-source community
- Growing awareness: 60,000 unique hits per month



Traditional design project (18 months)



Open-source model



Processor/Hardware evaluation based on:

- Available apps and device drivers
- Tools and debugging environment
- Standard open-source test suites

SW development entails:

- Obtaining device drivers from suppliers
- Build open-source applications
- Porting proprietary applications

www.blackfin.uclinux.org for more information

Blackfin Processor Development Tools

Development tools provide easier and more robust methods for engineers to develop and optimize DSP systems and shorten product development cycles for faster time-to-market. Components include:

- EZ-KIT Lite®**
 Desktop evaluation board includes an evaluation suite of VisualDSP++® development environment. The evaluation suite of VisualDSP++ has limited memory only.
- EZ-Extender®**
 EZ-Extender daughter boards give developers access and ability to connect various peripherals from Analog Devices and third parties to the expansion interface of the EZ-KIT Lite evaluation kits.
- EZ-Board™**
 The EZ-Board evaluation board provides developers with a low-cost platform for initial evaluation of the Analog Devices processors via an external emulator standalone debug agent board or uClinux®. Note: this board is not equipped with any JTAG debug interface. To debug you must have a [Debug Agent Board](#) and [Emulator](#). The EZ-Board has an expansion interface that allows for modularity with different EZ-Extender boards.
- Debug Agent Board**
 The Standalone Debug Agent is intended to provide a modular low cost emulation solution for EZ-Boards as well as evaluation boards designed by third parties. The standalone debug agent is very similar to the debug agent that is on existing EZ-KIT Lites but will have the flexibility to move from one board to another board.
- Starter Kit**
 Provides everything needed to get started on an application. Starter Kits contain a Blackfin EZ-KIT Lite, EZ-Extender daughter board(s), and the Software Development Kit (SDK) which contains sample code, "how to" documents, and various encoders/decoders that make getting started on an application easy and shorten the learning curve.
- Emulators**
 Rapid on-chip debugging allows developers to load code, set breakpoints, and observe variables, memory, registers, etc.



ADZS-BF518F-EZLITE



ADZS-BF548-EZLITE



ADZS-BF527-EZLITE

ADZS-ICE-100B JTAG Emulator

- **Supports ADI's Blackfin Processors (no SHARC support)**
 - PC to host interface is **USB 2.0**
 - Bus Powered
 - Plug-Fest certification pending
 - **Small Form Factor**
 - 3.0" x 0.78"
 - **IEEE 1149.1 JTAG Compliant**
 - **CE Certified**
 - **ROHS Compliant**





ADZS-ICE-100B Features

- Fully compatible with **VisualDSP++ IDDE** and **GDB** debug Interfaces
 - Complete debug capability including:
 - R/W memory and registers
 - Program download
 - Hardware and software breakpoints
 - Run, Step, Halt,
- Multiprocessor support
 - Synchronous run, step and halt
- 1.8V, 2.5V, and 3.3V I/O targets
- Download speeds of up to 250 Kbytes/sec
- Statistical Profiling and the Background Telemetry Channel are not supported



ADI Emulator feature comparison

	HP USB ICE	USB ICE	ICE 100B
Resale	\$4000	\$1200	\$150
Download Speed	1.5 MB/sec	150 KB/sec	250 KB/sec
Multiprocessor Support	YES	YES	YES
1.8, 2.5, 3.3V Compliant	YES	YES	YES
5V tolerant and 3.3V compliant for 5V processors and DSPs	YES	YES	YES
Supports all ADI Processors & DSPs	Blackfin/SHARC/TigerSHARC	Blackfin/SHARC/TigerSHARC	Blackfin only
Background Telemetry Channel	YES	NO	NO
Statistical Profiling	YES	NO	NO
CE Certified	YES	YES	YES
ROHS Compliant	YES	YES	YES



Blackfin Software Modules

Video/Imaging Decode

- JPEG Decoder
- MPEG-4 SP/ASP Decoder
- H.264 BP Decoder
- Windows Media Video (WMV9) Standard Decoder
- MPEG-2 Video Decoder

Video/Imaging Encode

- JPEG Encoder
- MPEG-4 SP/ASP Encoder
- H.264 BP Encoder

Audio Decoders & Post Decoders

- MP3 Decoder
- Windows Media Audio (WMA9) Standard Decoder
- MPEG-4 HE-AAC v2 Decoder with DAB Support (includes MPEG-4 HE-AAC v1 Decoder)
- MPEG-4 AAC-LC Decoder
- DTS Neo:6
- DTS 5.1 Decoder
- Dolby Digital (AC-3) 5.1 Decoder
- Dolby Headphone v2
- Dolby Virtual Speaker
- Dolby Pro Logic IIx Decoder

Audio Encoders

- MP3 Encoder
- MPEG-4 HE-AAC v2 Encoder
- Dolby Digital (AC-3) Consumer Encoder
- Windows Media Audio (WMA9) Standard Encoder

Post Processing

- Asynchronous Sample Rate Converter
- Enhanced Video Post Processing (eVPP)
- Multi-band Graphic Equalizer

Other Software

- Other software can be made available upon request software.module.request@analog.com





Requesting Software/Licensing

- **Customers can download many software modules from ADI's website directly to their machines**

- Uses click-through license agreement
- Not all software available for download, refer to SRF information below
- Some software modules time-out under evaluation license

<http://www.analog.com/en/embedded-processing-dsp/software-and-reference-designs/content/index.html>

- **Alternatively, request software using our on-line Software Request Form (SRF)**

- Includes complete list of standard software modules available from ADI
- Agreements sent directly to customer for their signature
- Latest updates & non timed-out versions available
- Code shipped directly to customer via FTP

www.analog.com/requestsoftware

Summary

- **The MCU and DSP selection process is inherently different**
 - Blackfin addresses the key criteria of both processes
- **Common features in Blackfin that are also common in MCUs**
 - Hierarchical memory, instruction and data caches
 - Memory management unit that offers user space and memory protection
 - A broad set of peripherals common in MCUs
- **Rich peripheral mix to provide system functionality at lowest BOM cost**
- **Numerous third-party tools and operating systems**

